FPGA-based Hardware Accelerator for PAPR Reduction Using UFMC Signal Precoding Technique with OpenCL

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Abstract. This research proposes a precoding technique to reduce the Peak-to-Average Power Ratio (PAPR) in Universal Filtered Multi-Carrier (UFMC) modulation systems implemented on a hardware accelerator based on Field-Programmable Gate Arrays (FPGAs) using Open Computing Language (OpenCL). High PAPR is a significant challenge in communication systems, as it directly affects the efficiency and linearity of power amplifiers, leading to signal clipping and a decrease in Bit Error Rate (BER) performance. To mitigate these effects, the original signal is multiplied by a Square Root Raised Cosine (SRC) matrix before being processed through the UFMC system. The methodology includes a theoretical analysis of PAPR and the SRC precoding technique, along with simulations and tests on the UFMC transmission system structure. Results indicate a significant reduction in PAPR, improving system efficiency and processing time without compromising signal quality or increasing computational complexity. This approach demonstrates that the proposed method is a viable solution for UFMC systems, optimizing energy efficiency and real-time performance for demanding applications, such as next-generation mobile networks.

Keywords: UFMC, Precoding, FPGA, OpenCL, Transmission

1 Introduction

Next-generation communication systems, such as 5G, demand high performance across use cases like Enhanced Mobile Broadband (eMBB), Ultra-Reliable Low Latency Communication (URLLC), and Massive Machine Type Communication (mMTC) [1]. Universal Filtered Multi-Carrier (UFMC) modulation has emerged as a promising candidate for these applications due to its advantages over traditional Orthogonal Frequency Division Multiplexing (OFDM) and Filter Bank Multi-Carrier (FBMC) schemes [2,3]. Unlike OFDM, which applies a single filter across the entire band and suffers from spectral leakage and timing synchronization issues, UFMC divides the spectrum into sub-bands and applies filtering to each, reducing spectral leakage and improving signal quality. This method offers a balance between the simplicity of OFDM and the subcarrier-level filtering of

FBMC, which, although precise, increases filter size and processing time, making FBMC less suitable for real-time 5G applications [4].

However, a common challenge faced by both UFMC and OFDM is a high Peak-to-Average Power Ratio (PAPR), which results from combining multiple subcarriers and creates amplitude peaks that can cause signal clipping when passing through nonlinear high-power amplifiers. This clipping not only degrades Bit Error Rate (BER) performance but also causes spectral spreading, leading to interference and reducing system efficiency. Simply forcing the amplifier to operate within its linear range is not practical due to energy efficiency concerns in mobile systems [5].

To address this, we propose a precoding technique that mitigates high PAPR by multiplying the original UFMC signal by a Square Root Raised Cosine (SRC) matrix before transmission [6]. This approach uses Open Computing Language (OpenCL) to make a FPGA-based hardware accelerator to enable parallel processing and optimize system performance in real time. The proposed solution reduces PAPR without compromising signal quality or increasing computational complexity, making it ideal for energy-efficient applications such as 5G/6G mobile networks.

This paper is organized as follows. Section II explains the proposed technique in detail. Section III presents the methodology. Section IV discusses the results obtained. Section V concludes the paper.

2 Technical Background

2.1 Definition of PAPR

Peak-to-Average Power Ratio (PAPR) is a critical metric in communication systems, particularly in multicarrier transmission schemes such as UFMC. PAPR is defined as the ratio of the peak power to the average power of a signal $x(t)$, and it can be mathematically expressed as:

$$PAPR(dB) = 10log\frac{max\left|x(t)\right|^2}{E\left\{\left|x(t)\right|^2\right\}} \tag{1}$$

To graphically illustrate the values of PAPR, the Complementary Cumulative Distribution Function (CCDF) is often used:

$$CCDF = Probability(PAPR \geq PAPR_0) \tag{2}$$

where $PAPR_0$ is a chosen reference level.

2.2 The SRC Technique

This precoding approach aims to reduce the PAPR, which is crucial for improving the efficiency and performance of communication systems. By using the SRC matrix, signals are better conditioned for transmission, thereby minimizing the impact of non-linear distortions caused by high PAPR values. The proposed technique involves multiplying the original signal by a Square Root Cosine (SRC) matrix of dimensions $L \times N$. The general form of the SRC matrix is given by:

$$\mathbf{P} = \begin{bmatrix} p_{0,0} & p_{0,1} & \cdots & p_{0,N-1} \\ p_{1,0} & p_{1,1} & \cdots & p_{1,N-1} \\ \vdots & & \ddots & \vdots \\ p_{L-1,0} & p_{L-1,1} & \cdots & p_{L-1,N-1} \end{bmatrix} \tag{3}$$

where $p_{i,j}$ are the elements of the precoding matrix, $L = N + N_p$ represents the total number of subcarriers, and N_p are additional subcarriers used for overhead, with $0 \leq N_p < N$.

Given an input vector x with N orthogonal subcarriers:

$$\mathbf{x} = [x_0, x_1, \cdots, x_{N-1}] \tag{4}$$

The output of the precoder can be expressed as:

$$\mathbf{z} = \mathbf{P} \times \mathbf{x} = [z_0, z_1, \cdots, z_{L-1}] \tag{5}$$

The elements of the matrix P are suggested to be:

$$p_{i,n} = p_{i,0} e^{-j2\pi \frac{in}{N}} \tag{6}$$

with:

$$p_{i,0} = \begin{cases} \frac{(-1)^i}{\sqrt{N}} sen\left(\frac{\pi i}{2N_p}\right) & 0 \leq i < N_p \\ \frac{(-1)^i}{\sqrt{N}} & N_p \leq i < N \\ \frac{(-1)^i}{\sqrt{N}} cos\left[\frac{\pi(i-N)}{2N_p}\right] & N \leq i < L-1 \end{cases} \tag{7}$$

The parameter β, known as the null variable, is defined as:

$$\beta = \frac{L-N}{N} = \frac{N_p}{N} \tag{8}$$

Given the number of orthogonal subcarriers N and the overhead subcarriers N_p, it is possible to define the matrix P. Additionally, it can be shown that P satisfies the orthogonality condition:

$$\mathbf{P} \times \mathbf{P^T} = \mathbf{I} \tag{9}$$

where I is the identity matrix of dimensions $N \times N$ and P^T is the transpose of the original matrix P.

2.3 The OpenCL Framework

OpenCL, developed by the Khronos Group [7], is an open standard for cross-platform parallel programming that supports a variety of computing platforms, including CPUs, GPUs, and FPGAs. Its unified programming model enables developers to write code that can be executed across different hardware types, facilitating the testing and simulation of designs on accessible platforms like CPUs and GPUs before deployment on specialized hardware such as FPGAs.

A key advantage of OpenCL is its flexibility and interoperability with other platforms. For example, its open-source nature allows for seamless integration with MATLAB [8], enabling OpenCL code to be executed directly within the MATLAB environment through function calls [9,10]. This capability significantly accelerates the development process, as it allows for rapid testing and validation of algorithms in a familiar setting before implementation on hardware.

In this work, OpenCL was utilized to run simulations on CPUs and GPUs, streamlining development and testing phases prior to the final implementation on FPGA. This approach is particularly beneficial since FPGAs offer high power efficiency and parallel processing capabilities, making them well-suited for the demanding throughput and energy constraints of 5G and 6G systems.

By leveraging OpenCL, the FPGA-based hardware accelerator can take advantage of features like loop unrolling and memory bandwidth optimization [1], allowing it to manage intensive signal processing tasks more effectively. The combination of OpenCL's platform heterogeneity and the energy-efficient architecture of FPGAs makes this setup an ideal choice for our application.

3 Methodology

For the development of this research, we utilized MATLAB along with the OpenCL Toolbox [9] to construct the UFMC structure illustrated in Fig. 1. This environment allowed for the simulation of the precoding technique and efficient testing of various parameters and configurations. The system employs Quadrature Amplitude Modulation (QAM) and a conventional UFMC modulator, in addition to a precoding block that utilizes OpenCL code to apply the SRC technique, simulating the FPGA-based hardware accelerator.

As Fig. 1 illustrates, random binary data is generated and mapped into QAM. These mapped data are then multiplied by the SRC matrix in the FPGA precoding block. OpenCL is used exclusively in this block, where the mapped data are sent to the kernel that executes complex matrix multiplication on the OpenCL device. After execution, the resultant signal returns to the MATLAB workspace as a new variable, allowing the flow of the UFMC system to continue normally. The precoded signal is then converted from serial to parallel format based on the number of sub-bands M, each containing N subcarriers. Next, an N-point Inverse Fast Fourier Transform (IFFT) is performed, replacing unallocated carriers with zeros. Considering $\mathbf{x_i}$ as the precoded signal, the output after the IFFT from each sub-band is given by:

$$\mathbf{y_i} = IFFT\left\{\mathbf{x_i}\right\} \tag{10}$$

The filtering is performed using a Dolph-Chebyshev filter, which is uniform across each sub-band. This filter applies a Dolph-Chebyshev window to the IFFT

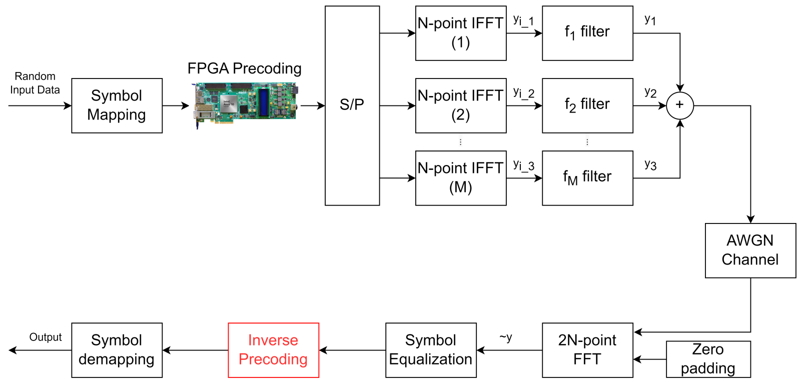

Fig. 1. UFMC Transceiver System

output to achieve the desired sidelobe attenuation. Consequently, the output for each sub-band after filtering is:

$$\mathbf{y} = \mathbf{H} \times \sim \mathbf{Q} \times \mathbf{y_i} \tag{11}$$

where H denotes the Toeplitz matrix with dimensions $(N + L - 1)$, and $\sim Q$ refers to the Inverse Fourier Matrix.

After filtering, the sub-bands are serialized again and sent through an Additive White Gaussian Noise (AWGN) channel. The receiver adds zero padding to create guard intervals between successive symbols, preventing Inter-Symbol Interference (ISI) caused by the inherent delay of the filter. It then applies a $2N$-point Fast Fourier Transform (FFT). The equation below represents the FFT output:

$$\sim \mathbf{y} = FFT \left\{ \left[\mathbf{y}^{\mathbf{T}}, 0, 0, \ldots, 0 \right] \right\} \tag{12}$$

Finally, the process of recovering the original signal includes equalization, inverse precoding, and symbol demapping.

4 Results and Discussions

To evaluate the effects of applying the SRC precoding technique, we simulated the traditional and optimized UFMC system in a MATLAB environment with OpenCL Toolbox. The initial parameters for these simulations are detailed in Table 1.

Figure 2 illustrate the Complementary Cumulative Distribution Function (CCDF) curves as the parameter β varies, which corresponds to an increase in the number N_p of overhead subcarriers.

The results show a clear reduction in Peak-to-Average Power Ratio with the application of the SRC precoding compared to the traditional approach. We

Table 1. UFMC System Parameters

Parameters	Values
FFT size (N)	512
Subband size	20
Number of subbands (n)	10
Modulation	QAM
Sidelobe attenuation	40 dB
Filter window	Dolph-Chebyshev
Filter size	43
Channel	AWGN
SNR	15 dB
Bits per symbol	4 (16-QAM)

see the minimum PAPR is observed at $\beta = 10\%$, reducing from 8.2379 dB in traditional approach to 5.7928 dB.

To assess the performance of optimized system under different numbers of subcarriers, we varied these parameters, and the results are depicted in Fig. 3. For these simulations, we set $\beta = 10\%$ as this represents a reasonable balance, effectively reducing the PAPR while avoiding a significant increase in the number of overhead subcarriers in the block.

The simulations reveal that even when the number of subcarriers per block is increased by a factor of 4, the variations in PAPR remain minimal. At a probability level of 10^{-2}, the PAPR for the UFMC system it is around 7 dB. These findings highlight the robustness of the SRC precoding technique in maintaining low PAPR levels across varying subcarrier configurations, demonstrating its effectiveness.

We examined the impact of the SRC precoding technique on the Bit Error Rate (BER) in Fig. 4 by comparing BER between traditional and optimized UFMC systems. For comparison, Fig. 4 also displays the theoretical BER curve for Quadrature Amplitude Modulation (QAM). The UFMC system shows a slight decrease in BER, suggesting a minor increase in system performance in terms of BER, as it achieves lower BER at a given Signal-to-Noise Ratio (SNR) compared to traditional method. These results indicate that SRC precoding technique does not significantly affect the BER for UFMC, demonstrating the inherent robustness of SRC precoding technique in maintaining lower error rates under similar conditions.

Finally, we evaluated the system processing time using MATLAB Profiler feature. We used the OpenCL Toolbox to simulate the entire system considering the precoding block and offload matrix multiplication functions to an OpenCL device. In order to compare performance on various computers with different CPU and GPU models, we tested the code execution on 5 computers, totaling 7 different OpenCL devices. Table 2 shows the results. It is noted that the execution time had an average of 1 second, with some computers achieving better performance compared to others. This is directly linked to the computational

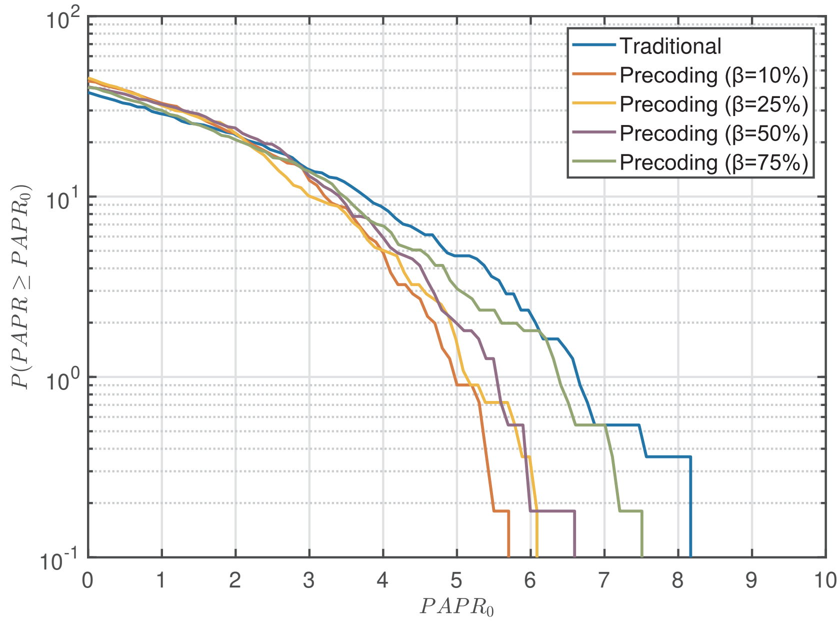

Fig. 2. UFMC System CCDF for different values of β

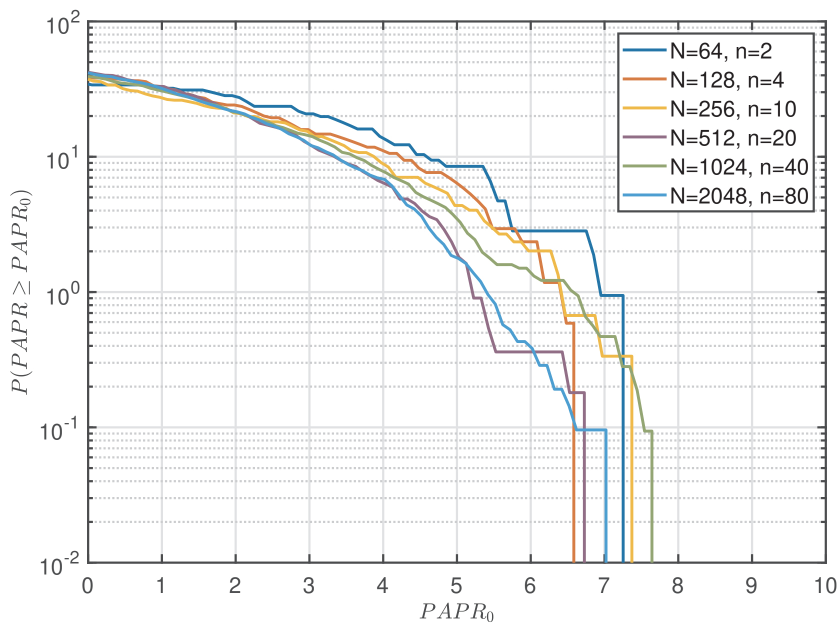

Fig. 3. UFMC System CCDF for different values of subcarrier number (N) and number of subbands (n)

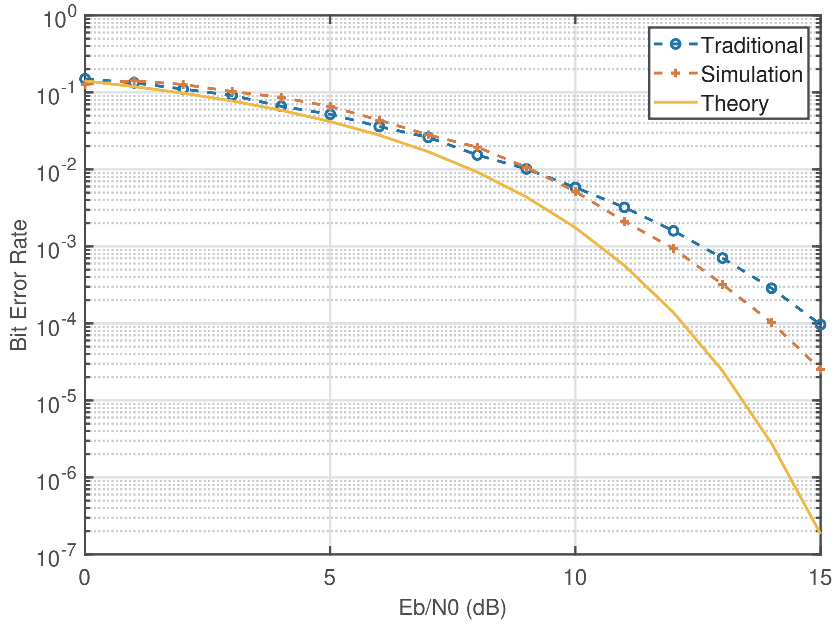

Fig. 4. Comparison among BER values for UFMC traditional and precoding and theory QAM (n)

power of each OpenCL device, which has specific characteristics such as parallel data processing rate, maximum sizes for local and global memory allocation, among other factors. It is worth mentioning that all OpenCL devices were sharing other functions with the computer besides precoding the UFMC signal, as they were not dedicated for do that. The implementation of an FPGA could allow its dedicated use for this function, further increasing the performance of the system as a whole.

Table 2. Performance Test

OpenCL Device	Execution Time [s]
AMD Radeon(TM) Vega 8 Graphics	0.476
Radeon 540X Series	1.551
Intel(R) HD Graphics 630	1.446
AMD Radeon R5 430	2.136
Intel(R) Core(TM) i7-7700 CPU @ 3.60GHz	0.378
AMD Ryzen 5 PRO 5650GE @ 3.40 GHz	0.519
NVIDIA GeForce® MX110	0.731

5 Conclusion

This study introduced an SRC-based precoding technique applied to multi-carrier modulation system UFMC, a contender for next generation 5G/6G networks. The primary objective was to reduce the high PAPR inherent in this system, which is a critical limiting factor for the performance of telecommunications signals.

Simulation results demonstrated that proposed technique effectively reduced the PAPR, achieving values close to those of single-carrier systems. The reduction led to a PAPR around 5.8 dB at the probability level of 10^{-2}. Regarding the Bit Error Rate (BER), the SRC precoding had minimal impact on UFMC, maintaining performance like the traditional system. The use of an OpenCL device allowed the system to offload precoding block function in a dedicated and parallel manner, reducing processing time.

In conclusion, the SRC precoding technique proved effective in reducing PAPR for UFMC systems used in 5G applications, with minimal impact on BER performance. This approach presents a promising solution for mitigating high PAPR issues in these multi-carrier modulation technologies, without significantly increasing the computational complexity of the system.

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