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An assessment of a Square-Wave Series Voltage Compensator increasing Low Voltage Ride Through capability on industrial electronic loads

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***Abstract*— This paper addresses a study of Dynamic Voltage Restorers (DVRs) and Series Voltage Compensators (SVCs) applied to voltage surge protection and able to maintain the voltage on susceptible loads. The restorer is applied on industrial environments when reliability of drives and electronics systems is desired, avoiding stops by voltage surges and problems from electrical grid, such as voltage sags. It is estimated that power quality problems generate production losses and downtime in manufacturing process at industries, in consequence of sensible loads to voltage variation, simplified solutions will be presented for this concern. First, the conventional sinusoidal dynamic voltage restorer will be cited, and then, three simplified topologies will be discussed, with the proposal of a square-wave series voltage compensator (SW-SVC) able to compensate voltage sags with improved cost-efficiency. The design includes a description of the inherent system parts, such as the coupling transformer, harmonic filter at the output of the static power converter, the converter configuration and its semiconductors, the input rectifier, grid synchronization system. Then will be discussed the performance analysis mitigating voltage sags, increasing Low Voltage Ride Through (LVRT) of electronic loads and improving industrial power quality.**

Keywords*— *voltage sag, power quality, PQ, dynamic voltage restorer, DVR, square-wave series voltage compensators, SW-SVC, Low Voltage Ride Through, LVRT.

I. INTRODUCTION

The electric power quality (PQ) is a concern for utilities and consumers, and it has been studied and harmful phenomena characterized as well as ways to mitigate them. The requirement is to provide consumers with energy of high reliability, according to standards and indicators. Voltage sag is one of these power quality problems, and it has been studied extensively for the last 23 years. It is characterized by a sudden decrease in the root-mean-square value of the supply voltage to magnitudes ranging from 0.1 to 0.9 p.u. in relation to nominal values, and lasting from 0.5 cycle to 1 minute, according to IEEE Std. 1159-2009, [1]. Research reveals that the main causes for voltage sag phenomenon are transmission system faults, remote distribution system faults, local distribution system faults, starting current of large motors, short interruptions and protections action, [2]. Regarding the causes of faults in the transmission and distribution systems, they can vary according to the local climate and transmission lines configuration. In European countries such as the United Kingdom, facility failures account for 39% of distribution system faults, grid interference 21%, atmospheric discharges 12%, snow and ice over the grid 11%, animals in contact 8%, strong winds 7%, and neighboring charges 2%, [2].

At tropical countries such as Brazil, the causes of faults are mainly due atmospheric discharges 21%, contact with trees and shrubs 16%, contact with animals 15%, grid failures 13%, human actions 6%, winds 5% and unknown causes 24%. The grid contact with trees and animals is due to the Brazilian transmission pattern, the grid is mainly placed by airways and bare conductors, [2]. The unknown causes for faults happen due to the distribution system size. Including a need for greater application of observatory process, that identifies such problems. In the United States, the conditions of adverse climate are mainly, being 62% of the causes, followed by problems on grid equipment 10%, contact with animals 7%, unknown 12% and maintenance 1%, [3]. Utilities, industries and consumers must be prepared to the adverse conditions that generate voltage sags, this phenomenon impacts causing defects in electronic equipment and financial losses and should be observed with the Industry 4.0 evolution because of the electronic equipment growing trend [4].

II. VOLTAGE SAG PROBLEMS

Voltage sags and interruptions lead to significant financial losses to residential, commercial and industrial consumers. In an industrial environment with a growing trend towards automation and controlled/interfaced devices, equipment such as contactors, personal computers (PCs), programmable logic controllers (PLCs), and adjustable speed drives (ASDs) are highly sensitive to voltage sags as organized in Table 1, [5]. With the advent of industry 4.0, concern about the protection of electronics tends to increase due to the enlargement of electronic devices in the industry environment, [4, 5].

TABLE 1. MOST COMMON REASONS FOR VOLTAGE-SAG-RELATED TOOL SHUTDOWN FOR 33 TOOLS TESTED, [5]

Voltage Sag Susceptibility Ranking	Weak Link	Overall Percentage
1	Protection circuits: Pilot Relay (33%) and Main Contactor (14%)	47%
2	DC Power Supplies: PC (7%), Controllers (7%), I/O (5%)	19%
3	3-Phase Power Supplies: Magnetron (5%), RF (5%), Ion (2%)	12%
4	Vacum Pumps	12%
5	Turbo Pumps	7%
6	AC Inverter Drives	2%

The vulnerability of some components to voltage sags or interruptions has motivated research institutes to perform compatibility tests with some electronic and electro-mechanical components that are built-in sub-parts of entire machines or tools. Some devices may fail, mal operate, or disconnected by a protection system when subjected to reductions in the voltage magnitude. This data has motivated original equipment manufacturer (OEM) to retrofitting practices, reducing components sensitivity to the power supply voltage variation. These measures may involve replace more sensitive components, revise components or apply new technologies that will improve the compatibility of machinery and tools, [4, 5]. The financial losses due to power quality is an imminent problem to the industrial sector. Some researches and standards propose statistical metrics estimating the cost of these energy quality events and identifying financial saving potentials associated with compatibility, [6-9]. In fact, for power quality solutions implementation, an initial capital investment is necessary. To know the financial advantages of this investment is necessary to understand the damages caused by voltage sag and interruptions. The financial return varies according to the industry's productive segment. Table 2 shows a data obtained from separate power quality studies conducted by Electric Power Research Institute (EPRI), and indicates power quality events, case reports from 20 different industries, [5].

TABLE 2. REPORTED COST PER VOLTAGE SAG EVENT DATA ACROSS INDUSTRY, [5]

No.	Productive Segment	Reported Cost	Service Voltage	Load
1	Semiconductor	$ 1,500,000	69 kV	25 MW
2	Semiconductor	$ 1,400,000	161 kV	30 MW
3	Semiconductor	$ 700,000	12.5 kV	10 MW
4	Metal Casting	$ 200,000	13.8 kV	16 MW
5	Chemical Plant	$ 160,000	12.5 kV	5 MW
6	Pulp and Paper Mill	$ 110,000	161 kV	100 MW
7	Aerospace Engine Machining	$ 100,000	13.8 kV	10 MW
8	Food and Bevarage	$ 87,000	12.5 kV	5 MW
9	Chemical Plant	$ 75,000	66 kV	3 MW
10	Chemical Plant	$ 75,000	66 kV	5 MW
11	Electronic Component	$ 75,000	12.5 kV	5 MW
12	Crystal Growth	$ 60,000	12.5 kV	1 MW
13	Chemical Plant	$ 46,000	66 kV	30 MW
14	Wiring Manuf.	$ 34,000	12.5 kV	2 MW
15	Chemical Plant	$ 18,000	12.5 kV	2 MW
16	Fibers Plant	$ 15,000	12.5 kV	1 MW
17	Paper and Packaging	$ 10,000	12.5 kV	4 MW
18	Plastic Bag Manuf.	$ 10,000	480 V	4 MW
19	Plastics	$ 7,500	12.5 kV	4 MW
20	Stainless Steel Manuf.	$ 5,500	12.5 kV	2 MW

The choose for the most viable power quality solution for different industrial segments, using the data in Table 2 it is necessary to calculate a Reported Cost per Load indicator. It is possible to notice that semiconductor industries have the highest value of financial loss per power demand, being around $60,000/MW, when submitted to voltage sags and interruptions. In this context, standards such as SEMI F47 have been developed with the semiconductor manufacturing industry support, proposing that better equipment design would offer a great solution for immunity against voltage sag problems. Analyzing the Report nº 2 of Table 2, a industry with equipment already in operation, it is possible to implement a industrial series voltage compensator for the entire facility, of medium and high industrial voltages, such as Dynamic Voltage Restorers (DVR) with nominal power close to 10 MVA, with a one year payback, considering 4 annual power quality events. Based on this voltage compensation strategy, considering DVR costs, installations and annual maintenance, at the end of three-years period, the total savings from the project has reached $ 10.9 million, [5, 8].

However, research indicates that deployments of distributed power quality solutions may be more cost-effective. A third solution would be installing voltage regulators and embedded compensators on the process tooling equipment in the facility. This strategy would employ solutions such as the Dip Proofing Inverter (DPI), Small Dynamic Sag Corrector (MiniDySC), Dynamic Sag Corrector (DySC) and Constant Voltage Transformer (CVT). This strategy includes low-voltage solutions installed at a facility bus or panel level, they are effective in protecting many sensitive loads at once. The solutions are low-voltage Static Series Compensation technologies (SSC), Uninterruptible Power Supply (UPS), Sag Ride-Through devices (SRT), the Active Power Flywheel Technologies, and low power DVRs [5]. The cost of these solutions can be justified based on the number of processes or machinery that will be protected, installed along the production line, using most robust components when feasible. Based on this voltage control solution, it is estimated that, the semiconductor plant would realize a saving around of $15.6 million by the end of the first 3 years, [5, 8]. Voltage compensations near sensitive loads are more cost-effective, [5,10]. In fact, by placing the voltage series compensators close to the susceptible loads, as shown in Fig. 1, the power levels of compensators is designed to primarily assist the susceptible loads, improving LVRT.

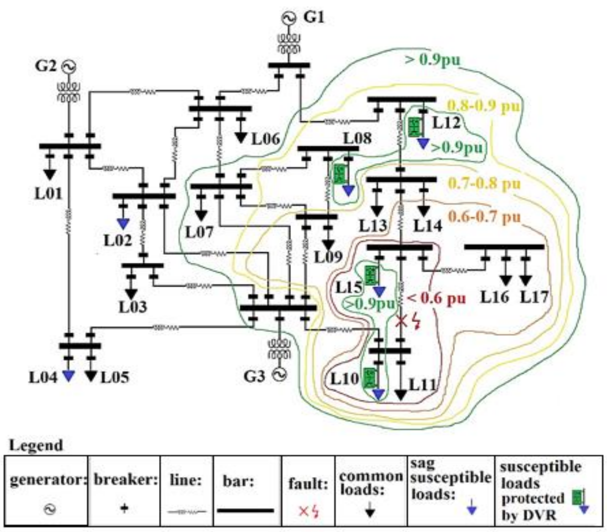

Fig. 1. Areas of vulnerability for loads connected to a grid under fault and susceptible to voltage sag.

There are computerized methods recognized that determine voltage sag magnitudes around the system for any fault location, when establishing the area of vulnerability it is possible to apply compensators close to the susceptible loads, [8, 11]. However, as proposed in IEEE Std. 1346-1998 voltage sag data is necessary to perform a compatibility evaluation with electronic process equipment, [8]. If measured data is not available, it is possible to install monitors and collect sag data, and the longer the data is collected, more reliable it will be. The same standard proposes a statistical study based on the summation curve of power quality events in an industrial plant or utility, to estimate the amount of annual events, voltage sags magnitude and duration. Collecting these data and the industrial equipment susceptibility graphic, it is possible to predict failures and establish strategies to increase the compatibility of machinery and tools, [8].

In a three-phase grid, sags can occur in one, two or three phases, and there may be irregular lag between phases. The sag are classified as type A, B, C, D, E, F and G, [2]. They are illustrated in Fig. 2 below. For sags that occur without phase jumps, it is possible to implement SVC as simplified and low cost solutions, objective of this work and discussed in the following sections. For phase jump sags up to a lag limit (3.4 degrees), agreeing with National Electrical Manufacturers Association (NEMA) and IEC 60034-26 standards, it is possible to use simplified SVCs solutions such as the quasi-sinusoidal SVC, [15]. The sinusoidal SVC is able to compensate for both scenarios, but the need for sinusoidal filters at the output increases cost, volume and complexity. Sinusoidal SVC inverters need to switch to frequencies in the order of kilohertz, while simplified solutions allow switching at the grid frequency, which improves electromagnetic compatibility, [15]. Fig. 3 demonstrates a voltage rectifier stage, quite common in electronic loads. This stage consists of a transformer that has the purpose to isolating the rectifier and the internal parts from the grid circuit, as well as adjust internal voltage levels. The DC bus of the rectifier stage has a capacitor adequately dimensioned to control the DC voltage ripple and is quite susceptible to voltage sag.

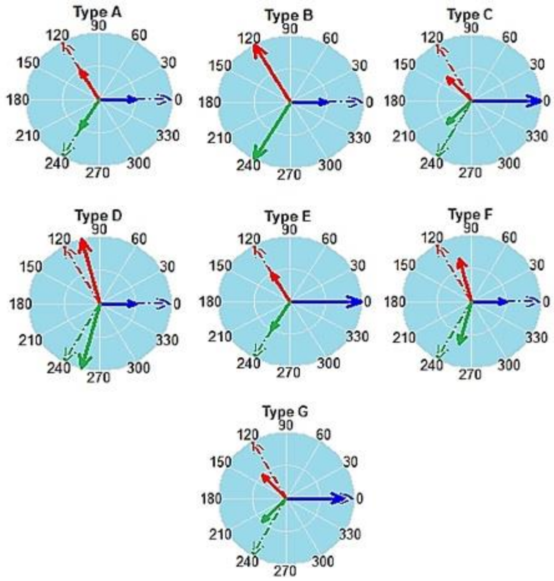

Fig. 2. Type of Voltage Sags.

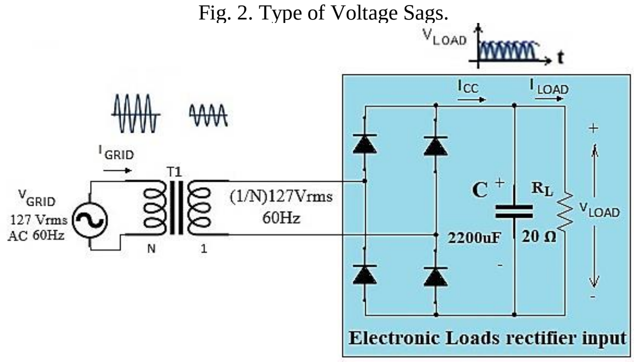

Fig. 3. Rrectifying load, typical input stage of electronic devices.

When partially discharged, the capacitor C causes under currents and under voltages in electronic devices, lowering useful voltages from the internal sources of the electronic equipment, damaging correct operation and power supply for integrated circuits (CIs), which may fail or shutdown. Fig. 4 below illustrates what happens internally with an electronic load when there is a residual 0.5 p.u. voltage sag in the grid. Electronic loads such as adjustable speed drives (ASDs), programmable logic controllers (PLCs), contactors and personal computers (PCs) that process and store data are subject to errors and damages during voltage sags, and are highly sensitive, [4,14]. In Fig. 4, for simplicity the transformation ratio was chosen $N = 1$. For a three-phase rectifier there must be a discussion about the susceptibility of the sensitive electronic load, which may be immune to a single-phase sag, because of voltage remaining in the other two phases. For simplicity, the circuit of Fig. 4 was chosen as a single-phase rectifier, and will be a study base for a low-cost SVC in the following sections, which can be placed only in the most susceptible phase of the system.

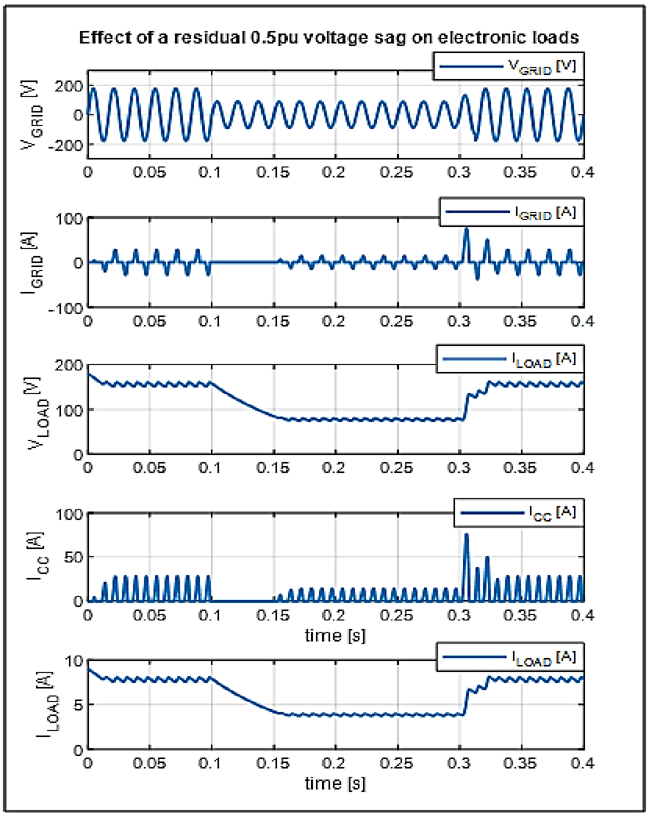

Fig. 4. Effect of 0.5 p.u. voltage sag on rectifier load, typical input stage of electronic equipment.

III. The Conventional Dynamic Voltage Restorer (DVR), with sinusoidal voltage compensation.

Fig. 5 shows a conventional DVR capable to provide voltage compensations in the sinusoidal form. When the impedance of the electrical system is low and the short-circuit current is much greater than the nominal current of the loads ($I_{SC}/I_N > 2$), the DVR input transformer ($T1$) is capable to drain a grid current charging the voltage restorer internal capacitor, by means of a rectifier stage. For the correct operation of this topology, a tuned control loop must control the DC bus voltage while another tuned control loop must act in synchronism with the grid voltage using a Phase Locked Loop (PLL). In addition, output filters are established, due to the need to mitigate harmonics from the frequency inverter, switched at high frequency (around $5\ kHz$ and $12\ kHz$).

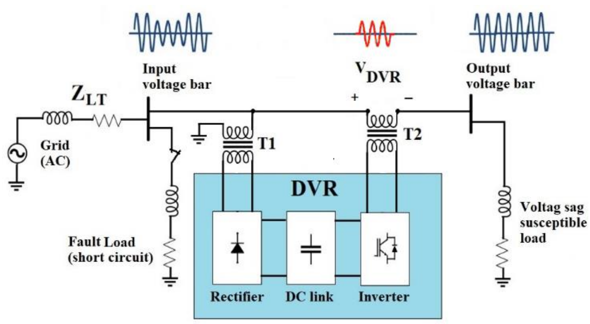

Fig. 5. DVR - Conventional Dynamic Voltage Restorer, sinusoidal voltage compensation

Fig. 6 is a more detailed explanation of the sinusoidal DVR, rectifier stage, PLL control loop, frequency inverter, output filters and grid coupling transformers. The DVR topology has been continuously explored, with component simplifications being a great research asset. The evolution in the SVC topology aims at the development of cost-effective solutions. The trend has been to migrate from topologies that use energy storage and series transformers and output filters, to topologies with shunt transformers combined with rectifiers that replace energy storage, and the energy for compensation is drained from the grid, [13]. Other evolution is substitution of the output filters, evolving to a voltage compensation performed with a grid frequency switching, [16,17]. The proposal in this work and explained in the following topics is a simplified square-wave series voltage compensator (SW-SVC), with is a DVR with improved cost-benefit to increase LVRT.

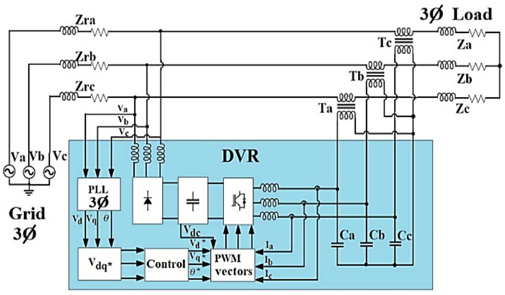

Fig. 6. DVR - Conventional DVR, sinusoidal voltage compensation, illustration of the control system, filters and grid coupling transformers.

IV. The square wave DVR with Cascade Cells – (SW-SVC - Topology A)

Fig. 7 shows a topology of a SW-SVC with Cascade Cells (Topology A). Its is a single-phase model, being a multilevel topology composed by cascade cells. The need for a multilevel topology is due to the different voltage sags levels, so the cells are used or placed in bypass according to the voltage magnitude to be compensated. The initial transformer stage of each cell suits the voltage levels, which will then be stored in the capacitor in the CC form. There is a concern for a project that is to define the number of voltage levels to be compensated, and this implies the number of cells and cost.

The international standard IEEE Std. 1250-2011 [9], indicates that the grid voltage levels must be between 0.9 p.u. and 1.05 p.u., for equipment safety and conformity. As shown in Table 3 below, a single cell with a transformation ratio of 1:0.2 is able to compensate 0.75 p.u. to 0.9 p.u. residual voltage sags. For a compensator composed of two cells with a transformation ratio of 1:0.2 and 1:0.6 it is possible to compensate from 0.5 p.u. to 0.9 p.u. residual voltage sags, which corresponds to the majority of cases being 80,5%, [16,17]. With these transformation ratio it is possible to synthesize levels of ± 0.2 p.u. (cell 1), ± 0.4 p.u. (cell 2-cell 1), ± 0.6 p.u. (cell 2), and ± 0.8 p.u. (cell 2 + cell 1) a linear combination can be established for the voltage compensation, according to (1):

$$v_{comp} = v_{sag} + a(v_{sag}) = v_{sag}(1 + a) \qquad (1)$$

Since the values for a can be (0.2, 0.4, 0.6 and 0.8), the possible values of for $v_{sag\ min}$ and $v_{sag\ max}$ are for $a_{max} = 0.8$ and $a_{min} = 0.2$:

$$v_{sag\ min} = \frac{0.9}{1 + a_{max}} = 0.5 \tag{2}$$

$$v_{sag\ máx} = \frac{0.9}{1 + a_{min}} = 0.875 \cong 0.9 \tag{3}$$

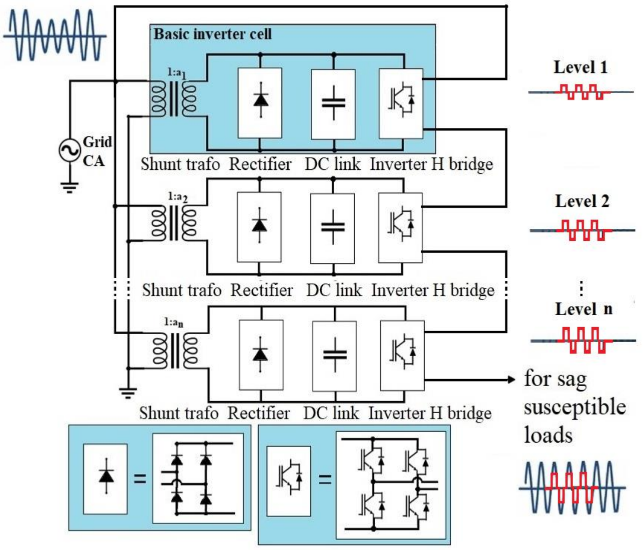

Fig. 7. SW-SVC with Cascade Cells (Topology A). Single-phase model.

TABLE 3. NUMBER OF CELLS VERSUS PERCENTAGE OF COMPENSATED VOLTAGE SAGS, [16]

Cell Num.	Transformation Ratio	Compensated Voltage Sag Range (p.u.)	Percentage of Voltage Sag Compensated
1	1:0,2	0,75 a 0,9	41,9 %
2	1:0,2 +1:0,6	0,50 a 0,9	80,5 %
3	1:0,2 +1:0,6 + 1x1:1	0,32 a 0,9	90,4 %
4	1:0,2 +1:0,6 + 2x1:1	0,24 a 0,9	93,5 %
5	1:0,2 +1:0,6 + 3x1:1	0,19 a 0,9	95,9 %
6	1:0,2 +1:0,6 + 4x1:1	0,16 a 0,9	95,9 %
7	1:0,2 +1:0,6 + 5x1:1	1,13 a 0,9	96,9 %
8	1:0,2 +1:0,6 + 6x1:1	0,12 a 0,9	96,9 %
9	1:0,2 +1:0,6 + 7x1:1	0,10 a 0,9	97,6 %

The increase in number of levels would bring higher costs to the equipment and would end up not adding a number of significant voltage sags. The two cell topology becomes the one with the most cost-benefit, compensating voltage sags from 0.9 to 0.5 p.u., when it varies from $P1$ to $P8$ in Fig. 8.

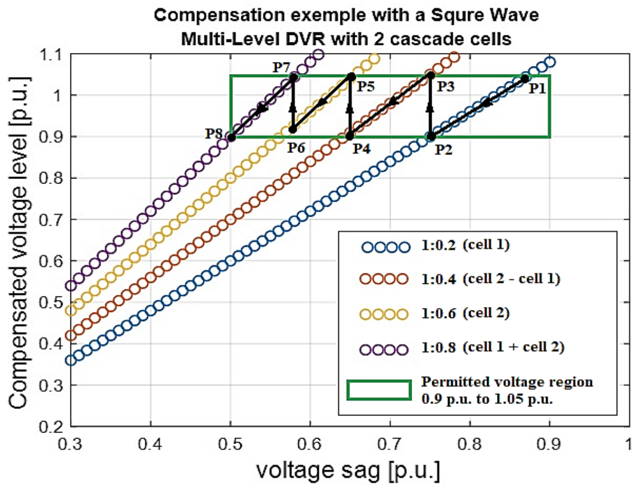

Fig 8. Compensation examples for SW-SVC - Topology A.

Fig 9 shows the three-phase version of the SW-SVC Topology A. As described, two voltage levels in square wave can be inserted and combined with each other, generating four resulting levels. Despite being a three-phase topology, the SW-SVC can be placed, by choice, on the phase most susceptible to voltage sags, [16].

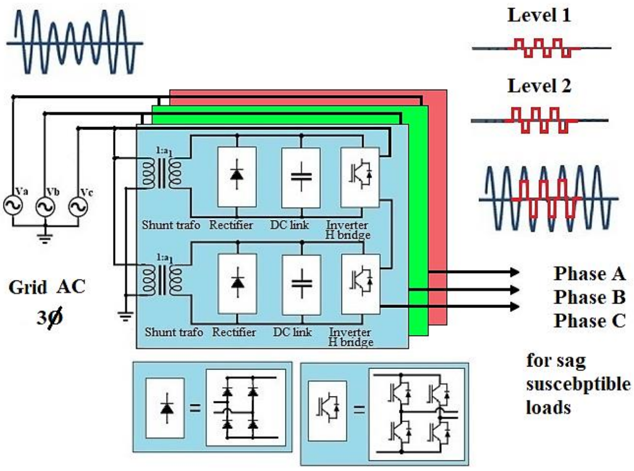

Fig. 9. SW-SVC - Topology A. Three-phase model with 2 cells per phase.

V. THE SQUARE WAVE DVR WITH CONTROLLED RECTIFIER BY TAPS SELCTION – (SW-SVC TOPOLOGY B)

In order to further simplify the square wave compensator of Fig. 9, the cascade cells may be modified by use of only one input transformer having voltage taps selected by controlled rectifier, as arranged in Fig. 10, [16].

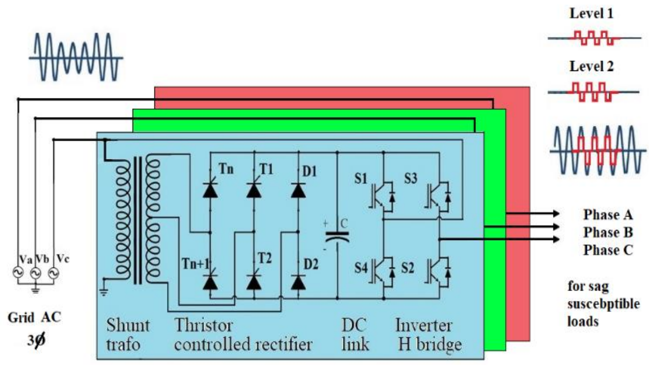

Fig. 10. SW-SVC - Topology B. Three-phase model.

The topology presented in Fig. 10 is a Multilevel SW-SVC selecting transformer taps by ccontrolled rectifier. The selected thyristor leg acts in synchronism with the diode leg which provides the capacitor charge at the voltage level suitable for voltage compensation. The H bridge compose of IGBTs couples capacitor charged to the grid. This means that in the positive half-cycle the capacitor is coupled to the grid in order to raise the voltage, and in the negative half-cycle the capacitor will be coupled to the grid in order to further reduce the voltage, restoring the grid RMS voltage. This topology has reduced number of components when compared to the SW-SVC topology A.

VI. The Square Wave DVRwith Controlled Rectifier by IGBT - (SW-SVCTopology C)

As a contribution of this article, an another SW-SVC topology is here presented. The SW-SVC topology B shown in the previous section becomes more cost-effective than the Topology A, and is therefore more promising. However, there is a concern about the taps choices of the topology B transformer. As shown in the previous sections, the choice of transformation ratio of each tap is intrinsically related to the compensated sag levels and therefore the compensator reachability. Depending on the choice of these values, the design may require a non-commercial shunt transformer, it must be purchased by commission and this tends to make the project a little more expensive. Simplifying the shunt transformer, a SW-SVC topology C is proposed and shown in Fig. 11. The thyristors and shunt transformers of the topology B were replaced by four diodes (D1 to D4) which form the input rectifier, and a nother IGBTs (S5) and one shunt transformer simplified. For high voltage topologies it would be possible to use GTOs instead of diodes, forming a controlled rectifier. For low voltage typologies, the IGBT S5 can be placed controlled the voltage level in the DC link, according to the sag severity. This topology can simplify the costs of the shunt transformer, enabling a simplified T1 transformer, with a ratio of even of 1:1.

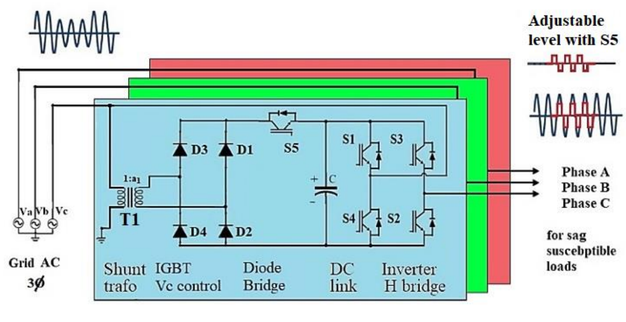

Fig. 11. SW-SVC - Topology C. Three-phase model.

VII. Simulated Results

The following simulated results will be presented for the three topologies of voltage series compensation in the square wave form. The topologies A and B, already existing and mentioned in previous articles, will also be evaluated for the voltage compensation on a rectifying load. The new topology C will have its performance evaluated and applied again to the same load type.

A. *The square-wave multilevel DVR with cascade cells - (SW-SVC Topology A)*

Fig. 14 shows the control system for the square-wave multilevel DVR with cascade cells - (SW-SVC Topology A). There is a voltage sag detection block, the grid voltage signal detection (synchronism system) and the gate drive required to switch the IGBTs. There is a "cell selection" block that has the logic addressed in Fig. 8 able to select switched or bypassed cells. Fig. 15 illustrates the simulated result for a 0.5 p.u. voltage sag restored.

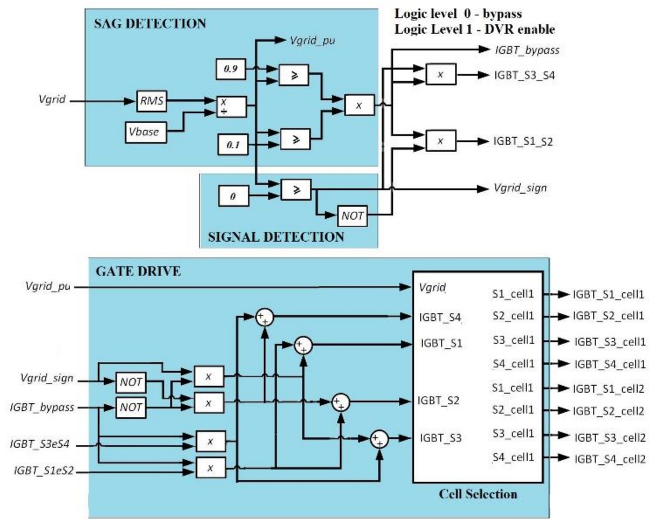

Fig. 14. Control scheme for square-wave multilevel DVR with cascade cells - (SW-SVC Topology A).

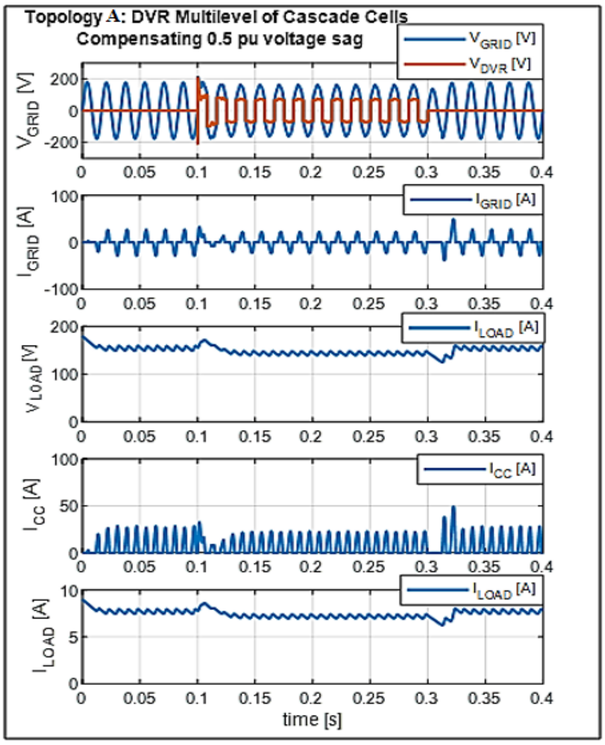

Fig. 15. A 0.5 p.u. voltage sag mitigation on rectifier load (electronic equipment) by square-wave multilevel DVR with cascade cells - (SW-SVC Topology A).

B. The square-wave multilevel DVR with controlled rectifier – (SW-SVC Topology B)

Fig. 16 demonstrate the control system for square-wave multilevel DVR with controlled rectifier - (SW-SVC Topology B). The "Tap selection" block selects the voltage level on the DC bus for correct compensation according to the voltage sag. The other blocks are similar to the previous control of Topology A, but now there is only one H-bridge of controlled IGBTs, per phase. Fig. 17 illustrates the simulated result for a 0.5 p.u. voltage sag restored.

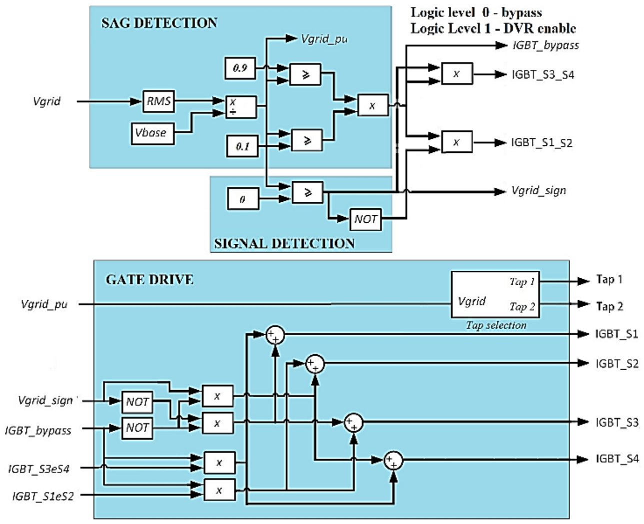

Fig. 16. Control scheme for square-wave multilevel DVR with controlled rectifier – (SW-SVC Topology B).

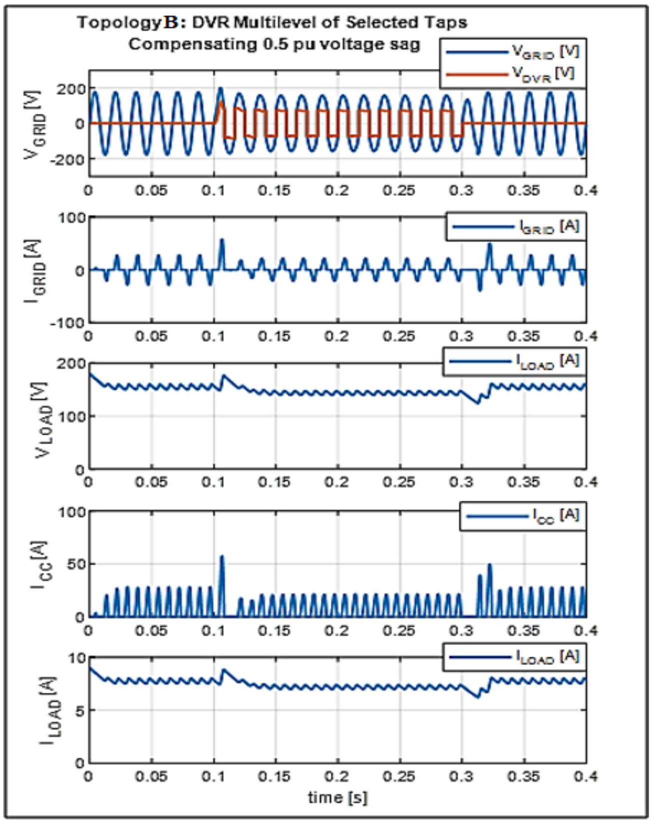

Fig. 17. A 0.5 p.u. voltage sag mitigation on rectifier load (electronic equipment) square-wave multilevel DVR with controlled rectifier – (SW-SVC Topology B).

C. The square-wave IGBT controlled rectifier – (SW-SVC Topology C)

Fig. 18 shows the control system for square-wave IGBT controlled rectifier - (SW-SVC Topology C). This topology features a 1:1 ratio shunt transformer. It is possible to compensate residual voltage sags up to 0.5 p.u. There is a hysteresis control that establishes in a linear way the DC bus capacitor voltage, no longer made by discrete levels. However, to establish this DC voltage, the converter switches back in 5kHz - 12kHz. The simplified transformer is a benefit.

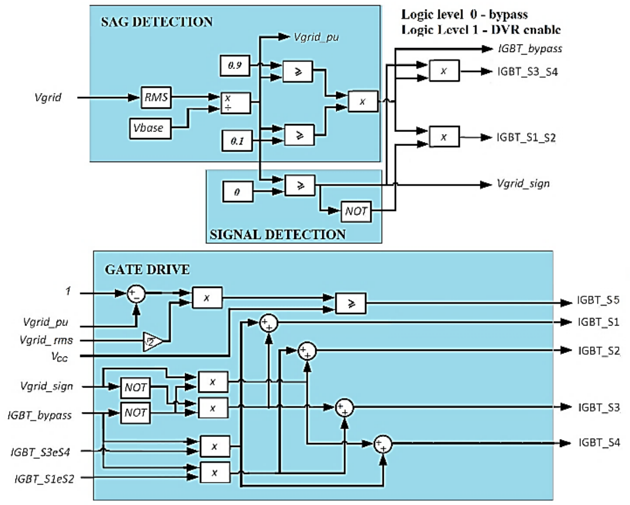

Fig. 18. Control scheme for square- wave IGBT controlled rectifier – (SW-SVC Topology C).

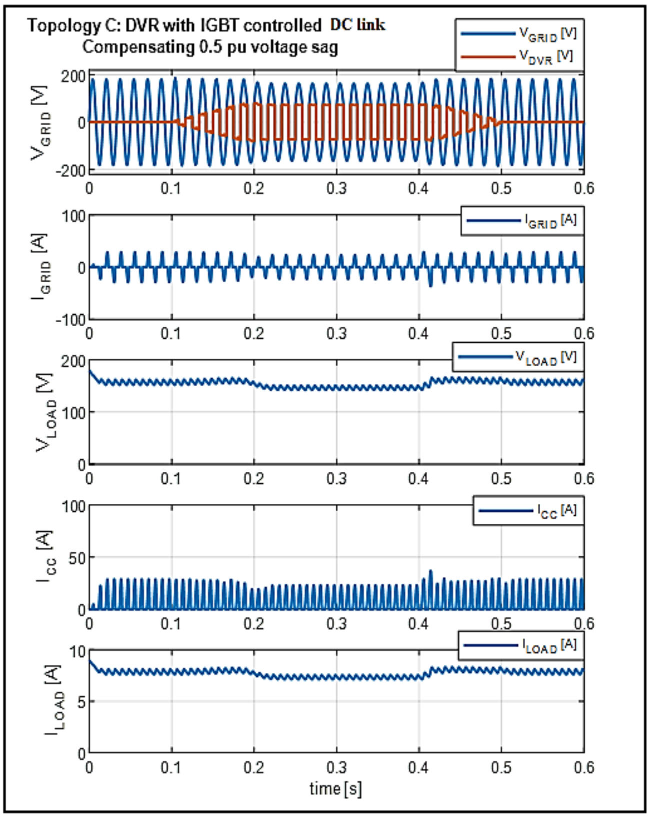

Fig 19. Topology A. 0.5 p.u. voltage sag mitigation on rectifier load (electronic equipment) square- wave IGBT controlled DC link – (SW-SVC Topology C).

VIII. Experimental Results

The SW-SVC Topology B was mounted on laboratory bench, as shown in Fig 20 and Fig. 21. It is designed to supply loads with 2 kVA power. Table 4 presents a list of the main components used for the topology test and Fig. 22 and 23 shows an already achieved experimental result, where there is a voltage sag compensation of 0.5 p.u. residual in an industrial electronic load.

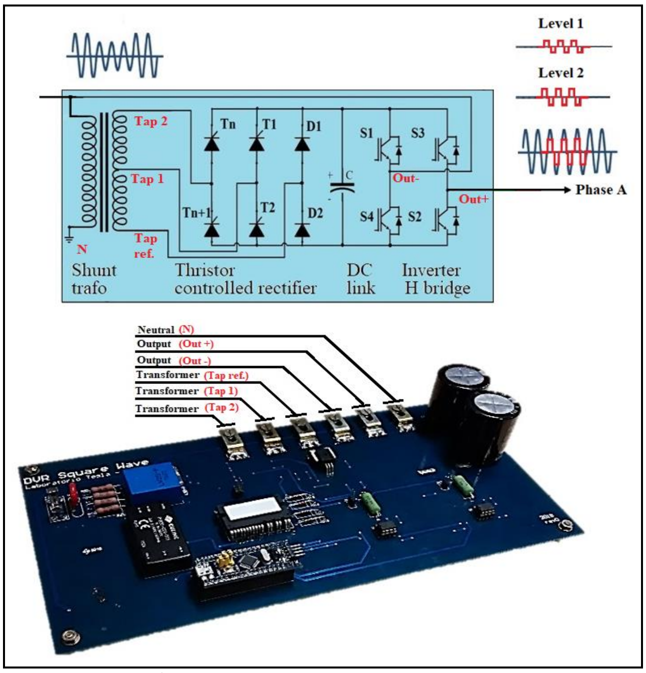

Fig. 20. Design of the square-wave multilevel DVR with controlled - rectifier (SW-SVC Topology B).

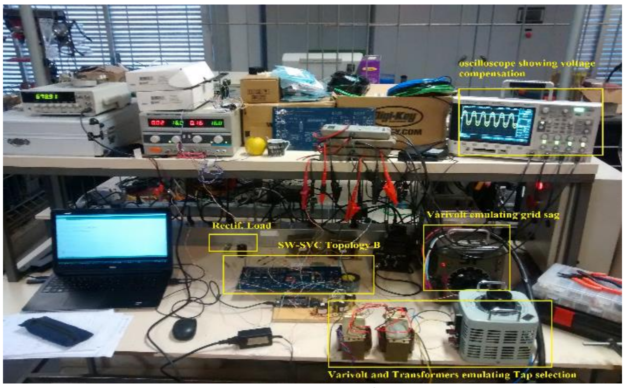

Fig. 21. Assembled laboratory bench for experimental results.

TABLE 4. MAIN COMPONENTS USED FOR TESTING SQUARE WAVE MULTILEVEL DVR WITH CONTROLLED RETIFIER (SW – SVC TOPOLOGY B)

Component	**Specification**
Shunt transformer	Transformation ratio 1:0,2 e 1:0,8
Thyristor	(4x) NXP Semicinductors BT152B_SERIES-351739
Diode leg	IXYS DSP8-08AS Standard Retifier Phase leg - 800V – 8A
DC link	(2x) Capacitor EPCOS EEE-FK1H151P 560μF / 400V
Inverter Bridge - H	FAIRCHILD FNE41060 Smart Power Module - 600V-10A 3-phase IGBT inverter bridge

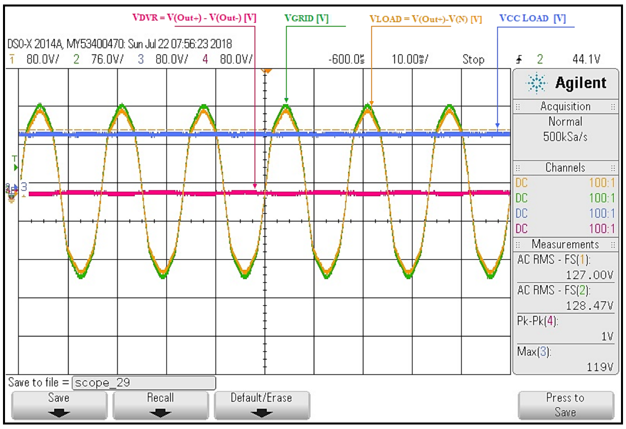

Fig. 22. Grid in correct operation. SW-SVC does not work and is bypassed.

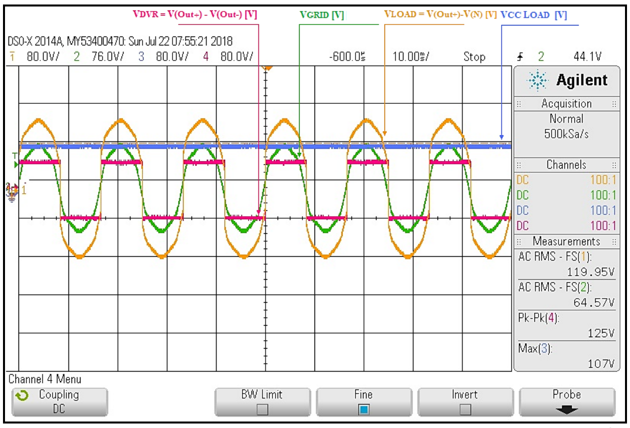

Fig. 23. Grid in 0.5 p.u. voltage sag. Voltage sag compensation on a rectifying load by square-wave multilevel DVR with controlled – rectifier (SW-SVC Topology B).

Fig. 22 shows the system in normal operation, when there is no voltage sag, the SW-SVC – Topology B is bypassed and the grid voltage appears at the output terminal. When there is voltage sag, the SW-SVC – Topology B selects the most convenient tap, loads its DC bus, and compensates with a square wave in series, as can be seen in its output terminal, the rectifier load DC voltage remains the same, Fig. 23.

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