Overview about Radiation-Matter Interaction Mechanisms and Mitigation Techniques

[1]Raphael R.N.S., [1]L. E. Seixas, [2]Agord M. Pinto Jr, [1]Saul A. Bascopé, [2]Leandro T. Manera, [1]Saulo Finco, [3]S. P. Gimenez

[1]*NCSH Department, Center of Information Technology Renato Archer CTI, Campinas, SP – Brazil*
[2]*FEEC Department, University of Campinas Unicamp, Campinas, SP – Brazil*
[3]*Electrical Engineering Department, FEI University Center, São Bernardo do Campo, SP – Brazil*
(e-mails: raphael.souza@cti.gov.br, luis.seixas@cti.gov.br, saulo.finco@cti.gov.br, sgimenez@fei.edu.br)

***Abstract*—This work presents a general overview about the origin and manifestation of ionizing radiation-induced effects over CMOS technology-based semiconductor structures. From the characterization of radiation-matter interaction mechanisms and effects, this work summarizes the set of design strategies described in the literature for radiation hardened electronic implementation, considering system level, block level and device level approaches. Additionally, a final case study is presented characterizing the Total Ionizing Dose TID tolerant operation of the Diamond MOSFET transistor as an innovative alternative of non-standard MOSFET's layout for space applications.**

Keywords— cosmic radiation effects; displacement damage; total ionization dose; single event effects; radiation hardening techniques; hardware redundancy; Diamond MOSFET.

I. INTRODUCTION

The development of electronic components and circuits associated with advanced mechanic systems allowed to explore the space above people's heads. Nevertheless, the launch of satellites over the atmosphere introduced to the science knowledge cosmic effects not observed at sea level. Much of the verified cosmic radiation is filtered by the atmosphere, but above it, satellite circuits are prone to suffer radiation interferences from a variety of sources (solar particles, galactic cosmic rays and magnetosphere) [1]. As a result, the set of radiation-induced effects from the interaction radiation-matter implies on the performance degradation of electronic devices through transient and fixed states.

Additionally, the CMOS technology down scaling contributes with the rising sensitivity of electronic devices (even for terrestrial applications) to radiation-induced performance degradation, especially considering structures for low power and high frequency applications [2][3][4]. This scenery establishes a research and development demand toward the proposition of effective solutions for mitigating radiation effects, according to acceptable limits [5][6][7] for each application.

From this application context, this work establishes a general overview about radiation effects on CMOS-based electronic devices. Thus, section II presents a brief description about ionizing radiation, section III presents a theoretical description about the physical effects from the interaction of radiation with semiconductors, and section IV summarizes the application of mitigation techniques for radiation hardened electronic design at system, topology and device level, in conformity with the nature of radiation-induced degrading effect. At the end of this section, a case study is presented considering the device level TID robustness performance of the Diamond MOSFET.

II. RADIATION: ORIGIN AND STRUCTURE

Considering the origin criterion, cosmic radiation can be categorized as extragalactic, galactic, solar, interplanetary or magnetosphere [1].

Produced by charged particles, electromagnetic radiation is physically described under a wave approach as a self-propagating synchronized oscillation of transverse electric and magnetic fields that propagate at speed of light in the vacuum. Under a corpuscular approach, it is composed by mass less particles or photons whose energy level is associated with the frequency. Considering the interaction with semiconductor structures, significant effects are verified from high energy (high frequency) radiation (x-rays and γ-rays) [1]. Particulate radiation is composed by matter units and elementary particles whose energy level is associated with mass and electric charge (protons, neutrons, electrons, positrons, ions and alpha particles) [1]. The main physical features of the radiation structure are summarized through the TABLE I considering 2 categorization criteria: mass and energy level.

III. IC RADIATION EFFECTS

Through direct or indirect physical mechanisms, the interaction radiation-matter involves different processes of energy transfer: atom displacement, nuclear reactions, decomposition of molecules and excitation/ionization of atoms [1]. The resulting effects are associated with the radiation features (mass, electric charge, energy level and incidence angle), and with the nature of the reference material (atom number and density). Thus, the verified set of interaction mechanisms is usually described considering 3 physical effects [6][7][8]: (1) Single Event Effects SEE, (2) Total Ionizing Dose TID, and (3) Displacement Damage DD.

The general features associated with each class of effect are summarized through the TABLE II, considering the time features of the interaction (single or cumulative), and the nature of the event (ionization or displacement).

TABLE I RADIATION: STRUCTURE AND FEATURES

Category	Mass less Particles	Massive Particles	
	Electromagnetic Radiation	*Charged Particles*	*Neutral Particles*
High Energy	x-rays	heavy ions	---
	γ-rays	alpha particles	
Low Energy	---	protons	neutrons
		electrons	

A. SEE Single Event Effects

Single Event Effects SEE represent a general class of random physical effects derived from the single incidence of high energy ionizing particles (protons, alpha particles, heavy ions) over semiconductor structures. According to the literature [9][10][11], a general classification can be defined considering the nature of the effects.

- **Hard Errors**: associated with permanent damages (from destructive effects).
- **Soft Errors**: associated with temporary damages (from non-destructive effects).

As an example, from the incidence of a high energy ionizing particle over the NMOS structure through the drain, according to Fig. 1, a general sequence of physical events can be characterized. Considering the mass, electric charge, energy level and incidence θ angle of the particle, different penetration paths can be established inside the semiconductor structure after collision. A set of electron-hole pairs is composed around the resulting penetration path, generating a distortion in the depletion layer of the drain-substrate junction around a funneling region, as illustrated in the Fig. 1. Thus, a sequence of 2 physical effects establishes in the drain a 2 components-based current pulse: (a) drift current generated by the electrons flow through the electric field in the drain and (b) diffusion current generated from the scattering of the remaining electrons in the substrate.

Considering the digital domain, the drift and diffusion effects-based current is a spurious current pulse characterizing a Single Event Transient SET effect (transient disturb on combinational structures) or a Single Event Upset SEU effect (static disturb on memory units) [10].

TABLE II RADIATION-MATTER INTERACTION PHYSICAL MECHANISMS

Features	Interaction		
	Ionization		Displacement
	Temporary	*Fixed*	*Fixed*
Cumulative Effects	---	TID	DDD
Single Event Effects	Soft Errors	Hard Errors	---

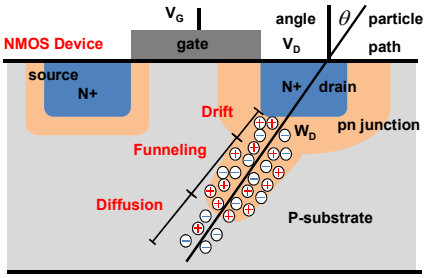

Fig. 1. Single Event Effects SEE: physical representation on device structure.

B. TID Total Ionizing Dose

Total Ionizing Dose TID represents a general class of ionizing-based cumulative physical effects derived from the continuous exposure of dielectric structures to low energy radiation [6][7][8].

Thus, from the distributed incidence of low energy radiation over a NMOS transistor through the gate, according to the Fig. 2, a sequence of resulting events can be described as follows: (a) incidence of ionizing radiation over the gate, (b) composition of a resulting set of electron-hole pairs in the gate oxide region, (c) migration of electrons through the channel electric field-induced drift current and (d) migration of holes toward the traps in the Si/SiO_2 interface region.

As a cumulative effect, the trapping of holes impacts on the electrical properties of the device, generating variations in the following parameters: threshold voltage V_{TH}, carrier's mobility, transconductance parameter, subthreshold slope, noise level and input capacitance.

C. DD Displacement Damage

Displacement Damage DD is a cumulative effect-based event generated from mechanical processes through the collision of particulate radiation (protons, neutrons, heavy ions, alpha particles or high energy electrons) with the silicon lattice, with the resulting displacement of atoms from the original position [12], as illustrated through the Fig. 3.

As a permanent effect, the resulting distortion on the silicon lattice can be characterized through the presence of vacancies (previous position of displaced atoms) and interstitial spaces (indicating new position after displacement), according to the Fig. 3(b).

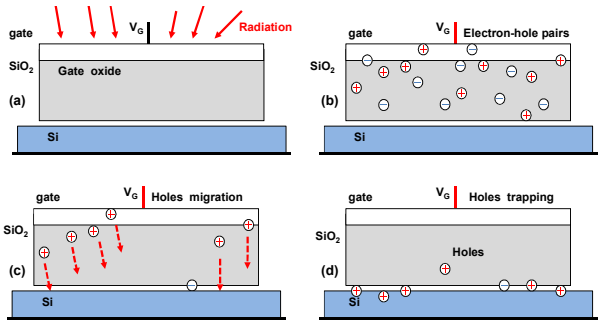

Fig. 2. TID: (a) radiation (b) electron-hole (c) holes migration (d) trapping.

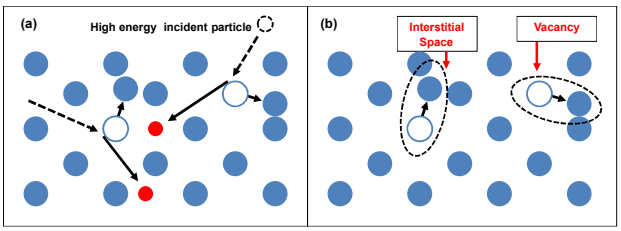

Fig. 3. DD mechanism: (a) incident particle and (b) lattice distortion.

IV. Radiation Hardened Design Techniques

A general criterion is usually defined for categorization of radiation hardening-based design techniques [6][13]:

- RHBP (Radiation Design by Process): implementation based on manufacturing process.
- RHPD (Radiation Design by Design): implementation based on design techniques.

In this context, a significant number of works has been proposed for describing RHBD-based design techniques for electronic structures implementation [13][14][15][16][17]. A general reference for robustness and reliability can be established from the following premises [18]:

- Simplicity: small amount of components.
- Robustness: components insensitivity to variations in the operation conditions.
- Redundancy: structure or behavior replication at system, block or device level.

Thus, from the referred design premises, the set of proposed radiation effects mitigation techniques can be summarized according to the general block diagram [13] in the Fig. 4. In this case, considering the nature of the physical effect and the particularities of the circuit or system for implementation, the design strategy to be applied involves the definition and sizing of structures in different design stages (schematic and layout), in different redundancy [16] domains (hardware, software, time and information) [13], according to the Fig. 4(a), and in different hierarchy levels (system, architecture, topology and device), according to the Fig. 4(b). On the other hand, the application of different rad-hard design strategies usually establishes a trade-off between the obtained radiation tolerance and the reference performance parameters as area, power consumption and noise level.

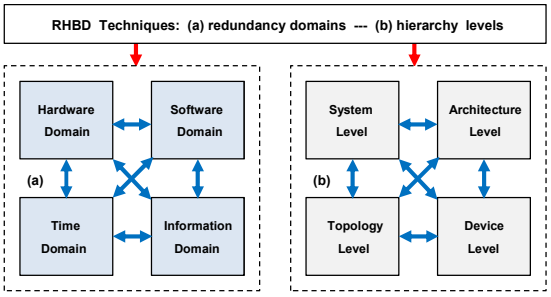

Fig. 4. RHBD design techniques: general diagram for categorization.

The next subsections present a general description about radiation effects mitigation techniques in different hierarchy levels for hardware redundancy-based applications.

A. System Level Techniques

System level methods for hardware redundancy-based design include different strategies for replication, [13][16] considering fault detection-based structures (Dual Modular Redundancy DMR), and fault masking-based structures (Triple Modular Redundancy TMR) [18][19][20][21][22].

As a primary concept for fault masking-based reliability, Triple Modular Redundancy TMR represents a particular structure of modular redundancy derived from the triplication of a given module. In this context, considered as black box, this module may represent different hierarchy levels in digital domain (logic gate, adder, or a complex digital system) or analog domain (delay cell in a ring oscillator). Thus, the collection of output data is provided from a voter circuit through the reproduction of the output generated from the majority of the modules, according to the Fig. 5. In this case, the resulting TMR network generates a correct output (without failures) even if one of the modules at most fails, assuming a not correlated operation between the modules [18].

From the analysis of the fault masking-based performance of a TMR network [23], the reliability model of the resulting redundant system R_S, disposed through TMR architecture, can be expressed as a function of the module reliability R_M, considering the voter reliability $R_V = 1$ (perfect voter) [18] [22][23], according to the equation in (1).

$$R_S(R_M) = 3R_M^{\,2} - 2R_M^{\,3} \qquad (1)$$

Thus, considering the Fig. 6(a), the resulting R_S variation profile is characterized with respect to R_M (in red), comparatively to an average straight line (in blue). In this case, the intersection point at P_E indicates an equivalent reliability level, and the subsequent data points indicate the R_M range with an effective reliability gain. Thus, an additional parameter can be defined for describing the effective average reliability gain G_R, according to the model in (2).

$$G_R(R_M) = \frac{R_S}{R_M} = 3R_M - 2R_M^{\,2} \qquad (2)$$

As result from this parameter, an additional variation profile can be characterized according to Fig. 6(b), indicating a maximum point in the curve at $P_M(R_M = 0.75, G_R = 1.125)$ for a given module reliability $R_M = 0.75$.

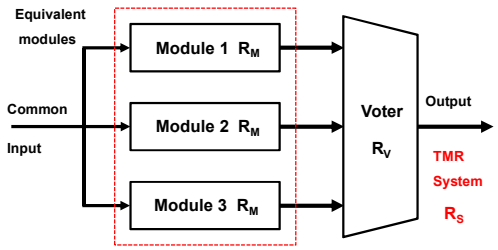

Fig. 5. TMR Triple Modular Redundancy: conceptual representation.

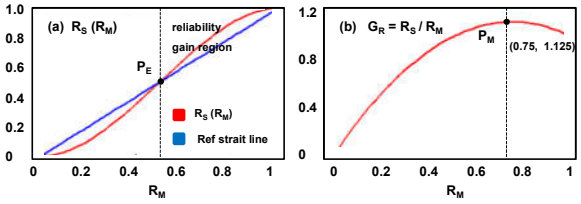

Fig. 6. TMR-based curves: (a) realiability R_S, (b) reliability gain G_R.

Alternative approaches for TMR-based systems have been proposed considering the impact over the area, power consumption and design complexity and, in this context, architectural variants from the reference TMR structure include proposals as Cascaded TMR [24][25], Hybrid Modular Redundancy HMR [26], and Hierarchical TMR [27].

B. Block Level Techniques

Considering hardware redundancy-based techniques [16], block level strategies for Single Event Effects SEE tolerant structures involves the replication of components according to different patterns. Toward this end, different approaches have been reported through the literature involving Quadded Logic [28][29], Interwoven Logic [30], and Dotted Logic [31].

Additionally, design techniques for TID tolerant structures include topology strategies for reduction of threshold voltage variation ΔV_{TH} effects. As an example, Fig. 7(a) illustrates a standard CMOS inverter and Fig. 7(b) characterizes the corresponding transfer curve considering the normal inverter operation (green line), an intermediary distortion state (blue line) and a higher distortion level after irradiation (red line). Resulting from V_{TH} reduction for NMOS devices, V_{TH} increase in module for PMOS devices, and increase in the current leakage I_{LEAK}, TID-induced distortion effects in the transfer curve of logic gates imply in a reduction of the output rail and variation in the switching point (Fig. 7(b)) [17].

A components replication-based strategy is illustrated from the Fig. 8(a), as a topology proposal for an inverter logic gate implementation [17]. This building feature provides additional components for compensating the threshold voltage variation in the both NMOS and PMOS transistors [17], for allowing a transfer curve with lower distortion levels, as indicated in the Fig. 8(b). On the other hand, this topology pattern implies on a comparatively higher input capacitance and reduced speed performance, considering devices with the same sizing.

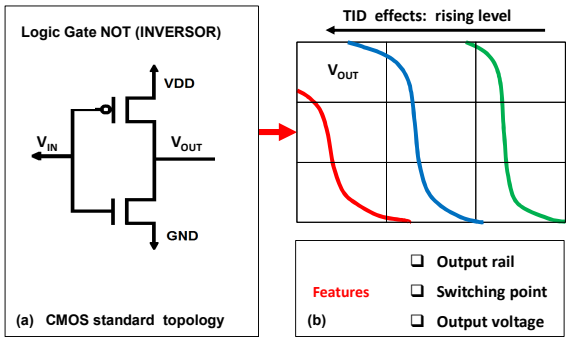

Fig. 7. Standard CMOS inverter: (a) topology (b) distorted transfer curve.

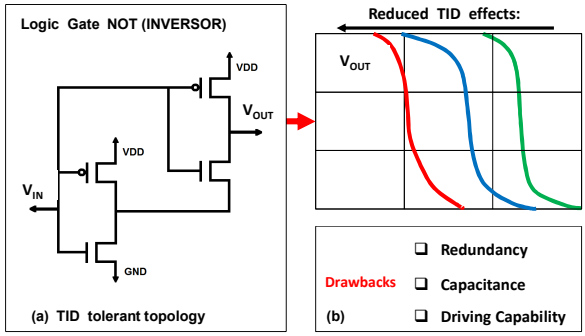

Fig. 8. Rad-hard CMOS inverter: (a) topology (b) resulting curve.

C. Device Level Techniques

From device-based hierarchy level, design strategies for radiation hardening usually involves a proper selection of (1) device geometry or layout style and (2) sizing techniques [32].

In this context, considering the first method, mitigation effects of the Total Ionizing Dose TID can be obtained through the current leakage reduction by applying enclosed layout devices geometries.

Resulting from the continuous incidence of ionizing radiation over the MOS gate structure, the presence of positive charges or holes accumulated in oxide traps (gate oxide and field oxide) and Si/SiO_2 interface traps generates current leakage I_{LEAK} by attracting negative carriers and creating a source-drain parasitic path in parallel with the device channel.

Considering the conventional layout transistor or conventional rectangular MOSFET (CM) represented in top view in the Fig. 9(a), the thick oxide in touch with both source and drain creates an inversion layer in the nearby region, generating 2 main leakage paths: intra-transistor and inter-transistor. Thus, from the representation of the side view of the conventional transistor (CM), Fig. 9(b) illustrates the trapping of positive charges in the bird's beak region, at the transition between the gate thin oxide and the field thick oxide, and the resulting migration of negative carriers (for composing the parasitic path).

In this context, considering the building features of devices with edgeless structure or annular gate shape [33][34][35], as represented in the Fig. 10, the bird's beak region involves a common voltage node, allowing a reduction in the edge current leakage. On the other hand, the drawbacks of this edgeless structure include the drain-source asymmetry (considering the area surrounded through the gate), increased capacitance and area, difficult to implement smaller levels of W/L ratio without enlarging L, and not availability for application in sub-100 nm technologies.

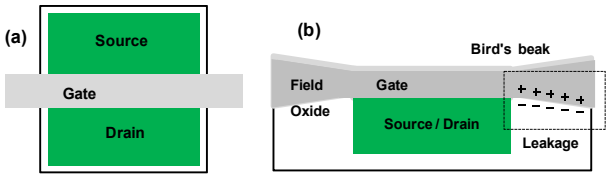

Fig. 9. Conventional transistor layout: (a) top view (b) side view.

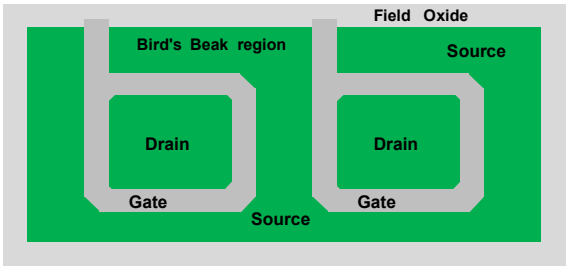

Fig. 10. Enclosed layout transistor ELT: top view.

Additionally, a more advanced approach for current leakage reduction through device level TID tolerant structures, considers non-standard gate geometries without requiring additional costs in the manufacturing process, by applying octagonal [36] and hexagonal (Diamond) patterns [37][38][39][40][41]. The application of the referred gate geometries implies on additional effects in the device operation as the DEactivation of PArasitic transistors in the Bird's Beak Regions (BBR) Effect (DEPAMBBRE) [40][41], allowing an improved and stable electrical performance for a wider temperature range [42][43][44].

Thus, for a given channel width W, a comparative illustration is indicated through the Fig. 11, considering the conventional layout transistor or conventional rectangular MOSFET (CM) with a channel length L, according to the Fig. 11(a), and the Diamond MOSFET (DM) [45], with the shortest and longest channel lengths b and B, respectively, according to the Fig. 11(b).

In this context, considering the devices in biased condition, E_0 indicates the vector representation for the longitudinal electric filed LEF in the CM transistor (Fig. 11(a)), and E_T indicates the resulting LEF in the DM transistor, considering the vector components E_1 and E_2 for a given α angle of the hexagonal gate geometry (Fig. 11(b)). In this case, for a common state of biasing and sizing condition (channel width W and aspect ratio W/L) for the both devices, the resulting DM LEF tends to be comparatively higher than the CM counterpart, considering the Longitudinal Corner Effect LCE [40][41].

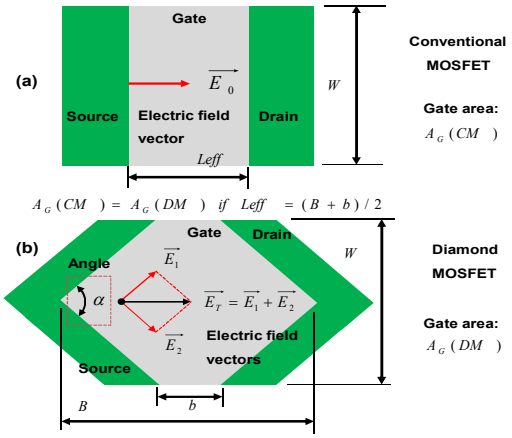

Fig. 11. Transistors top views: (a) CM and (b) DM.

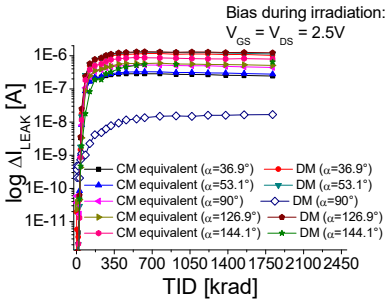

Fig. 12. Current leakage ΔI_{LEAK} variation profile as a function of the doses.

For performance verification effects from a set of DM devices with different angles (α = 36.9°, 53.1°, 90°, 126.9° and 144.1°) and a given bias condition (V_{DS}=V_{GS} = 2.5 V), Fig. 12 characterizes the current leakage variation ΔI_{LEAK}, considering a ^{60}Co (standard) source radiation for a reference dose variation range. Thus, the corresponding curves indicate a current leakage reduction in DM devices with the increase in the α angle and, in this case, the lowest ΔI_{LEAK} level was obtained for α = 90^0 due to the DEPAMBBRE Effect [40][41].

V. Conclusions

Driven through the semiconductors market expansion, CMOS technology down scaling has represented one of the main bottlenecks for the electronic development, considering the new paradigms of operation for each technology node: reduced area and cost, decreased power, and higher performance. On the other hand, this process implies in a set of degrading factors as short channel effects, increased noise levels, process variation and radiation effects sensitivity.

Thus, from a radiation effects sensitivity-based approach, this paper presented a general description about the concepts involving the interaction radiation-matter, the set of interaction patterns (SEE, TID and DD) and resulting effects, and a general overview about mitigation techniques in different hierarchy levels (system, topology and device).

Through the application of RHBD-based techniques, several mitigation strategies can be applied in different domains: hardware, software, time and information. In this context, each method for radiation hardened design can be applied for comprising a given radiation-induced effect (SEE or TID), in a given hierarchy level and according to the requirements of each application.

Different approaches for hardware redundancy-based techniques has been proposed and validated comparatively to TMR-based faulting masking techniques for mitigation of SET-induced transient effects. Additionally, device level techniques have been described considering alternative non-standard gate geometries for MOS structures implementation, for allowing the improvement of TID robustness performance.

Finally, considering the analyzed case study, the application of Diamond MOSFET DM (α = 90^0) proved to be an innovative and effective solution for improving the TID tolerance performance for operation of electronic systems in space applications.

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