FPGA Implementation of a Lock-in Amplifier

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***Abstract*— This paper presents a digital Lock-in amplifier for extracting a signal of interest out of a noisy environment, using the synchronous frequency and phase-sensitive detection techniques. For this purpose, an FPGA was used because it has a large flexibility in the adaptation of digital filters. An analog-to-digital converter is also used with high resolution and low noise signals acquisition.**

From the results obtained, we consider that the developed equipment is suitable for use in several applications, including photoconductivity meters with low current values.

Keywords— Synchronous Detection, Phase Sensitive, Digital Filters, Embedded Systems.

I. INTRODUCTION

Lock-in amplifiers are synchronous demodulators and allow to accurately measure small AC signals in the presence of interference with noise in orders much greater than the signal amplitude. Synchronous demodulators use phase sensitive detection (PSD) to isolate the signal component at a specific reference frequency and phase. Any noise that is not on the same frequency and phase of the signal will be easily rejected without significantly impairing the measurements [1].

There are some works that proposed digital lock-in amplifiers using FPGA. In [2], a digital phase-sensitive detector (DPSD) for electrical impedance tomography was realized with a hybrid system using DSP, field programmable gate array (FPGA) chips and other analog circuits. Measurements on a saline filled tank show that the signal-to-noise ratio (SNR) of the system can be up to 60 dB.

In [3] is proposed the design and realization of a digital lock-in amplifier devoted to high-performance photon counting applications based on a PSD section implemented in an FPGA device. The experimental test of the instrument was performed by generating a signal with extremely low photon rates and a high background level with the aim to verify the high rejection of extremely low-frequency background fluctuations, and also the expected SNR with respect to the gated mode lock-in. The prototype has been experimentally tested and the results fully comply with the goal design specifications.

In [4] is proposed a monolithically integrated low-power dual-lock-in amplifier with integrated photodiodes. The waveforms were generated by two synchronized fast-gigabit (GX) serializers using FPGA. The measurement results show that a dynamic range of 27 dB could be achieved at a modulation frequency of 10 MHz.

Vandenbussche et. al. (2014) [5] investigate the possible causes of inaccuracy in a phase measurement system implemented using a digital lock-in amplifier architecture and using FPGA. They conclude that when phase measurement systems are used with low signal-to-noise ratio (SNR) signals, the low-pass filter in the lock-in amplifier plays a critical role in the overall accuracy of the system whereas for applications with a high SNR the analog to digital converter is the major contributor to the overall measurement inaccuracy.

A block diagram of the proposed measurement system is shown in Figure 1. The basic concept of a synchronous demodulator is that a sensor should be modulated by a provided reference output. The addition of this excitation signal for a sensor to measure a physical parameter moves to a frequency band that presents less noise. A carrier signal f_{REF} excites an external sensor at a specific frequency defined by the type of experiment. This causes a frequency shift of the physical parameter, measured by the sensor, to the frequency of the carrier. The band-pass filter (BPF) removes part of the noise that is outside the signal band.

A. Phase Sensitive Detection

The PSD technique is used to separate the signal of interest from the undesired. This is composed by a multiplier and a low-pass filter (LPF). The signal in the output of the multiplier is the product of the reference signal and the output of the filtered sensor. If the reference signal is sinusoidal, the physical parameter constant and there is no noise in the system, the signal at the output of the BPF would be expressed as:

$$V_{BPF} = V_B \sin(\omega_{REF} t + \varphi_B) \tag{1}$$

The multiplier output will be:

$$V_{mult} = V_B \sin(\omega_{REF} t + \varphi_B)\, V_{REF} \sin(\omega_{REF} t + \varphi_{REF}) \tag{2}$$

$$V_{mult} = \frac{1}{2} V_B V_{REF} \cos(\varphi_B - \varphi_{REF}) - \frac{1}{2} V_B V_{REF} \cos(2\omega_{REF} t + \varphi_B + \varphi_{REF}) \tag{3}$$

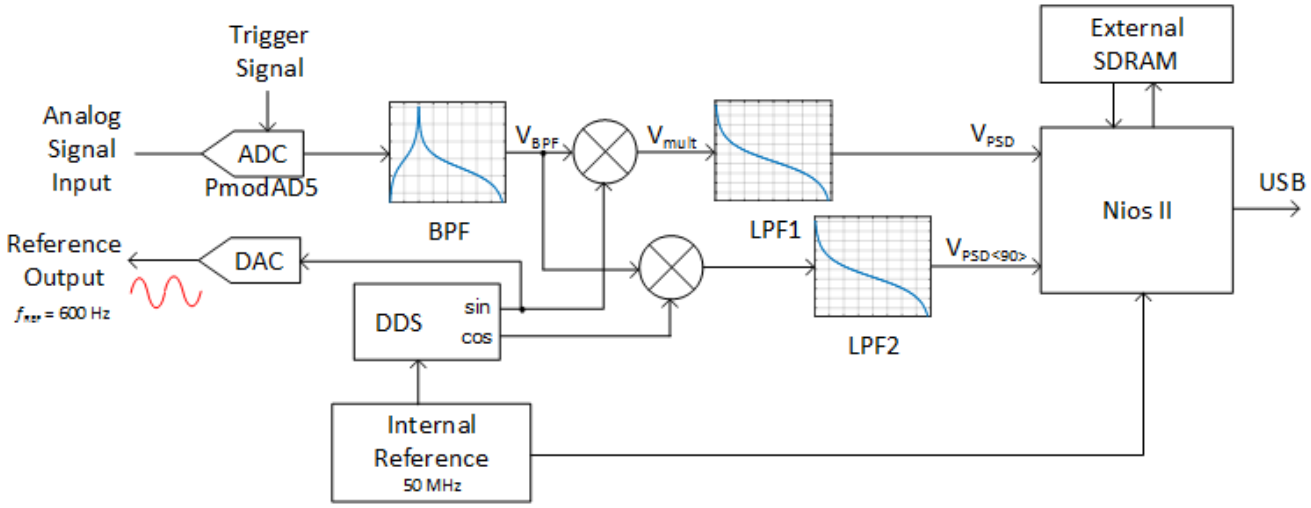

Fig. 1. Digital lock-in amplifier FPGA-based.

This is composed by a DC and an AC component which has the double of the reference frequency. In case that cut-off frequency of LPF is enough to remove the AC component, the output signal will be:

$$V_{PSD} = \frac{1}{2} V_B V_{REF} \cos(\varphi_B - \varphi_{REF}) \quad (4)$$

This DC signal at the output is proportional to the amplitude and phase of the measured signal. When the amplitude is kept constant, the LPF output can be used to measure the phase difference, and when the phase is held constant, it can be used to measure the amplitude variation. It should be noted that the reference signal does not necessarily need to be pure sine, but the excitation signal and the demodulation signal must share the same frequency and phase so that the PSD technique can be applied.

B. *Narrow Band Detection*

The PSD only detect frequencies very close to the reference frequency of the Lock-In. Assuming that the input is composed of noisy signal, noises with frequencies distant from that reference will be attenuated at the output of the PSD by the LPF filter. Noise with frequencies very close to the reference will be present at the output of the PSD with very low AC frequencies. A narrower bandwidth for the LPF will remove the sources of noise very close to the reference. The bandwidth of the LPF is also responsible for determining the lock-in amplifier detection band.

C. *Reference Frequency*

The carrier frequency will be the same as the lock-in reference ($\omega_B = \omega_{REF}$). In addition, the phase difference between them must also be constant in time, otherwise the result $\cos(\varphi_B - \varphi_{REF})$ will oscillate and will no longer be a DC signal. The reference of the lock-in amplifier must be synchronized in phase with that of the measured signal. In this project, direct digital synthesis (DDS) was used to generate the reference clock.

D. *Magnitude and Phase*

The PSD output is proportional to the signal $V_B \cos(\Delta\varphi)$, where $\Delta\varphi = \varphi_B - \varphi_{REF}$ is the phase difference between the sensor signal and the reference oscillator of the lock-in amplifier. When the reference phase φ_{REF} is set, $\Delta\varphi$ can be obtained equal to zero and consequently one can measure V_B (where $\cos\Delta\varphi = 1$). However, if $\Delta\varphi = 90°$ then it will not be possible to measure. A single-phase lock-in amplifier, with only one PSD, is used to measure only the real component of the measurement.

This phase dependence can be eliminated by adding a second PSD with a reference offset by 90° (cosine function). Then, the measurement after the BPF will be:

$$V_{BPF<90°>} = V_B \sin(\omega_{REF} t + \varphi_B + 90°) \quad (5)$$

And the output after the PSD in quadrature will be:

$$V_{PSD<90°>} = \frac{1}{2} V_B V_{REF} \sin(\varphi_B - \varphi_{REF}) \quad (6)$$

Considering the two outputs, in phase and in quadrature, it is possible to measure the components of the same signal through the relation:

$$V_X = V_B \cos(\varphi_B - \varphi_{REF}) \quad (7)$$

$$V_Y = V_B \sin(\varphi_B - \varphi_{REF}) \quad (8)$$

The magnitude and phase also could be computed as follow:

$$R = \sqrt{V_X^2 + V_Y^2} \quad (9)$$

$$\theta = \arctan\frac{V_Y}{V_X} \quad (10)$$

The value of R measures the amplitude of the signal and does not depend on the phase between the carrier of measured signal and the reference source of the lock-in amplifier.

II. METHODOLOGY

A. FPGA Architecture

For the signal processing was used a BeMicro MAX 10 Evaluation Kit from Arrow Electronics company, which has an Altera MAX 10 FPGA with 8k LEs, on-chip RAM, user flash memory and non-volatile autoconfiguration [6]. The kit also has an external memory of 8 MB SDRAM and is extensible via Pmod header digital interface.

For the acquisition of signals the Digilent PmodAD5 board was used, which contains an AD7193 analog-to-digital converter (ADC) with SMA connections for differential analog channel input [7,8]. The FPGA was used to implement digital filtering, data transmission via USB communication and also to control the ADC through SPI communication. A VHDL code was written to instantiate the components and make the complete system synthesis, likewise to define the input and output interfaces of the system on chip. In addition, a Nios II soft-core processor was implemented in FPGA to control SDRAM, implement SPI protocol, JTAG UART core, and including the mapping of registers and declarations in software for access to hardware.

The software development was carried out using standard ANSI C language and the Altera HAL system library.

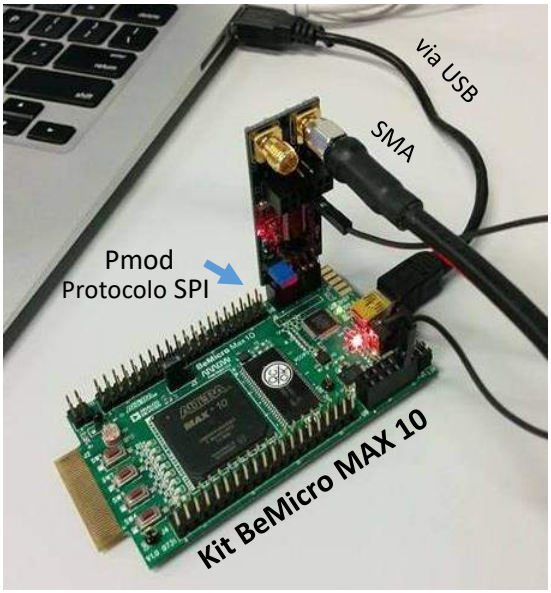

Fig. 2. Using the Pmod board for analog signals input.

B. A/D Converter

The ADC used in this project, AD7193, contains a fourth-order Σ-Δ modulator with 24-bit resolution and typically is used in applications that require high-precision measurements with rms noise as low as 11 nV, up to 22 noise-free bits (for unit gain configuration), operating input voltage range of ± 2.5 V in bipolar or 0 to 2.5 V in unipolar operation, and finally output data rate of 4.8 kSPS. The ADC is controlled and configured by its on-chip registers via 4-wire SPI serial interface.

The Σ-Δ modulator is an oversampling architecture. It uses digital filtering and decimation techniques to remove the quantization noise in the Nyquist band. With the noise transfer function modeling feature, quantization noise from the analog-to-digital conversion is modeled by the modulation scheme being shifted from a low band to higher frequencies. This allows a low-pass digital filter to eliminate quantization noise from conversion results. This means that the ADC Σ-Δ can be designed with the background noise determined only by the temperature noise, not being limited by the intrinsic quantization noise of the sampling process [9].

C. Altera Design Tools

The Quartus II tool was used for the analysis, synthesis, positioning and routing processes. Also, it allowed to compile the hardware design, described in Verilog and VHDL, generating the binary files and programming the FPGA.

Through Modelsim one can write a testbench script to automate the simulation of a project and its behavior. It reads some signal input stimuli at runtime, and checks the outputs in the specific blocks.

The QSys tool, which runs on Quartus II, allows the design of an embedded soft-core processor in FPGA, called Nios II. Interfaces with this processor can be set to be external to the FPGA chip, such as peripherals and memories controllers, or connecting to the internal logic system designed in HDL. The soft-core processor can be programmed in C language using open source IDE Eclispe and allows more advanced FPGA applications such as embedding Linux or mounting TCP/IP Ethernet protocol stacks, for example.

The SignalTap II Embedded Logic Analyzer is a debugging system-level tool that captures and displays the real-time signals on input and output pins of the FPGA using its internal resources. It is possible to analyze the behavior of the hardware (such as peripheral registers, memory buses, signals generated by the SPI protocol or for DDS synthesis, and other internal components of the chip) [10].

III. RESULTS

The signal of interest to be measured here is the photocurrent produced by a photorefractive crystal under illumination. Therefore, the analog current signal must be first converted into a voltage signal using a front-end transimpedance operational amplifier. After that, a trigger signal is required to enable A/D conversion in Pmod. The measurement signal goes through a passband filter, and then detection in phase and in quadrature are performed. The DDS will generate sine and a cosine (shifted by 90°) references for PSDs. Finally, the Nios II processor will do the calculations of magnitude and phase of the measurement signal. In the following sections this project will be presented in detail.

A. A/D Resolution

The AD7193 has up to 22 noise-free bits for the unit gain setting. Considering this sampling, the amount of multilevel quantization can be calculated as $M = 2^{22} = 4{,}194{,}304$ levels. The range of the voltage amplitude at the ADC input will

be $-2.5\,\mathrm{V}$ up to $2.5\,\mathrm{V}$ for bipolar operation. With this, the voltage resolution will be $1.192\ \mu V/\mathrm{level}$.

In order to establish the SPI communication with ADC was written a firmware in C language. In addition, the SignalTap II Logic Analyzer was used to monitor the signals generated in the interface pins, using as trigger reference the falling edge of chip select signal which should go to low state when transmitting or receiving data via SPI protocol.

Therefore, to allow communication with the chip registers it is always necessary to first send a word to a communication register. After that, it is possible to check the status of the ADC, modify the operating mode (use internal or external clock, make the measurement average, select which digital filter to use sinc^4 or sinc^3 [11], and determine the data rate of output), configuration (enable high chop data rate, differential analog or pseudo-differential input, select and Multiplexing the input channels, using buffer, gain PGA, etc.) and also read data. To reset the ADC and return all registers in the default configuration, one must write 40 bits '1' to the communication register consecutively.

B. Model Simulation

The proposed model to simulate the behavior of a lock-in amplifier, for later implementation in hardware, is presented in Figure 3. A reference frequency f_{REF} modulates a sensor, which measures a physical parameter, with a sine function. This same generated signal is used in the synchronous detection of PSD in-phase, and after a 90° phase-shift, a quadrature reference cosine is also generated. White noise is added to the signal amplitude during measurement. After passing through the BPF, the resulting baseband signal is demodulated in phase V_X and in quadrature V_Y components.

The sampling rate for the simulated digital model was $f_S = 4.8$ kHz and the generated sine frequency $f_{REF} = 600$ Hz.

The white noise source uses Gaussian distribution to generate random real numbers with zero mean and variance equal to 1. Discrete solver was used for the simulation.

Figure 4 shows the bandpass filtering of the measured signal on the sensor with additive white noise in amplitude. The BPF is centered on modulation frequency of f_{REF} sensor and already eliminates much of the noise spectrum, but it is not able to eliminate noise in that same frequency range. For this reason, the in-phase and quadrature PSDs are used, as the signals shown in Figure 5, which also considers a phase difference of $\Delta\varphi = 45°$ between the reference for the PDSs and the modulation signal for the sensor only as an example. Actually, could be any other value of $\Delta\varphi$ for the magnitude R measured to remain correct.

As can be seen in Figure 5 (c), the magnitude of the measured value is attenuated by $1/2$ due to the operation of the PSD (equation 4). This amplitude must be compensated in the algorithm.

C. Digital IIR Filters

Infinity impulse response (IIR) filters were implemented by the Butterworth method. Figure 6 shows the responses of the filters in dB and Table 1 shows the detailed parameters for the design of digital bandpass and low pass filters.

From the MATLAB toolbox Filter Design HDL Coder™ were generated the hardware description codes in Verilog for implementation in FPGA. The simulation of the filters was done using ModelSim through stimuli generated by Simulink's own scheme and verified the behavior of the hardware to evaluate the operation.

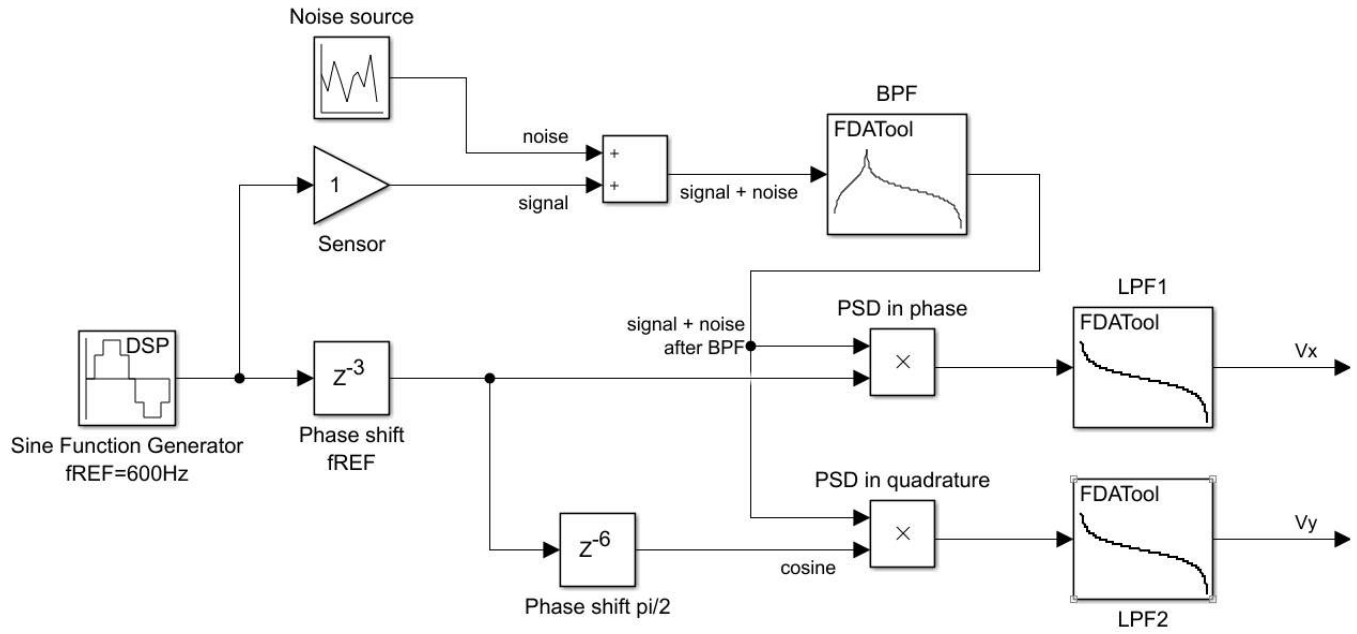

Fig. 3. Simulation model on Simulink environment.

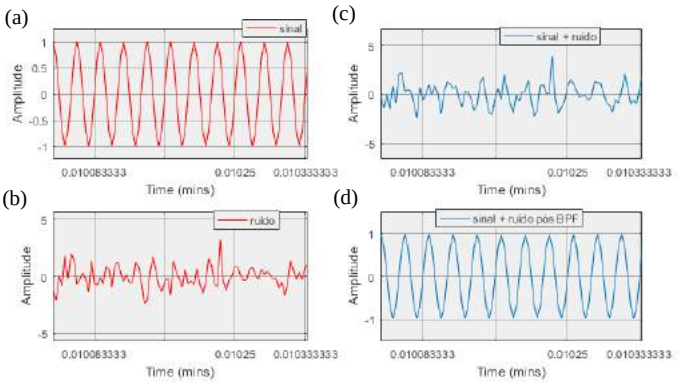

Fig. 4. Bandpass filtering. (a) Signal at $f_{REF} = 600$ Hz, after the modulated sensor. (b) White noise in Gaussian distribution. (c) White noise added to the signal amplitude. (d) Resulting signal after BPF IIR digital filter.

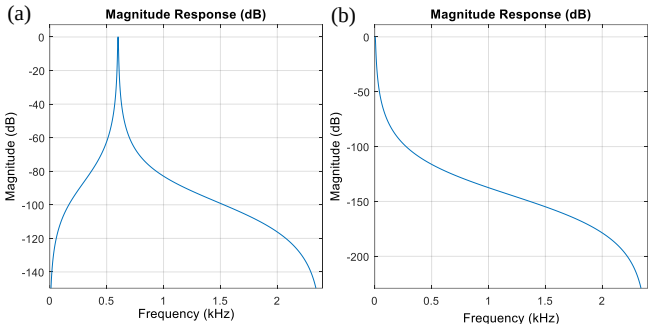

Fig. 6. IIR filters response. (a) BPF and (b) LPF.

TABLE I. IIR FILTERS SPECIFICATIONS.

	Band pass Filter (BPF)		***Low pass Filter (LPF)***
Order	4		3
Struct	Direct-Form II, second order sections		
Sections	2		2
Stopband	500 Hz	700 Hz	60 Hz
Passband	598 Hz	602 Hz	4 Hz
Sampling rate	4,800 Hz		
Bandpass Magnitude	1 dB		
Stopband Magnitude	60 dB		

D. Direct Digital Synthesis

Direct Digital Synthesis (DDS) is a type of frequency synthesizer used to create arbitrary waveforms from a clock reference in a digital system. For DDS we used an Altera's IP Core called NCO Compiler [12], which is a numerically controlled oscillator. Its simplified diagram can be presented according to Figure 7. In this step, the idea is to generate the sine and cosine functions inside the FPGA. Through SPI communication with a digital-to-analog converter (DAC), it is possible to use this signal to modulate a sensor as the reference frequency to measure physical parameters.

Fig. 5. Signal recovered by lock-in amplifier with the presence of white noise in the amplitude and considering a phase difference $\Delta\varphi = 45°$ between f_{REF} reference for PSDs and f_{MOD} modulation for the sensor. (a) V_X in phase, (b) V_Y in quadrature, (c) magnitude R and (d) phase θ.

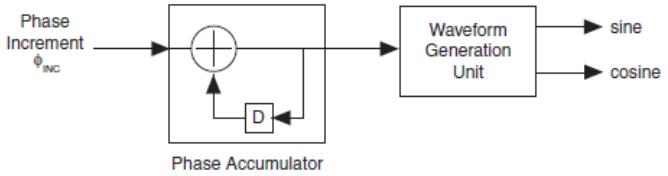

Fig. 7. Numerically controlled oscilator (NCO), adapted from [12].

The waveform of the sine generated follows the equation:

$$S\,(nT) = A\sin(2\pi f_o\, nT) \tag{11}$$

The accuracy of the phase accumulator set was 32-bits, with 16-bits angular resolution and 18-bits for magnitude resolution. The system clock frequency, quoted earlier in the BeMicro kit specification, is $f_{CLK} = 50$ MHz. The output frequency can be calculated by:

$$f_o = \frac{\varphi_{INC}\, f_{CLK}}{2^M} \tag{12}$$

The phase increment value (φ_{INC}) is provided by the software and depends on the desired output frequency. In this case, for $f_o = 600$ Hz we get $\varphi_{INC} = 51540$.

E. Gateware HDL

The complete system's Register-Transfer Level (RTL) diagram is shown in Figure 8, and was generated by Quartus II after compilation by the RTL viewer tool. All these components were instantiated in VHDL gateware for synthesis, routing and positioning of resources and generation of the binary file for FPGA configuration. The BPF, LPF1 and LPF2 filters were designed in Verilog HDL. For the sin_gen DDS block, the NCO Compiler IP Core was used, and for the nios_system cpu, Qsys was used in order to control external memories SDRAM and SFlash, control the Pmod interface, buttons, LEDs and perform calculations after conversion and Filtering of signals.

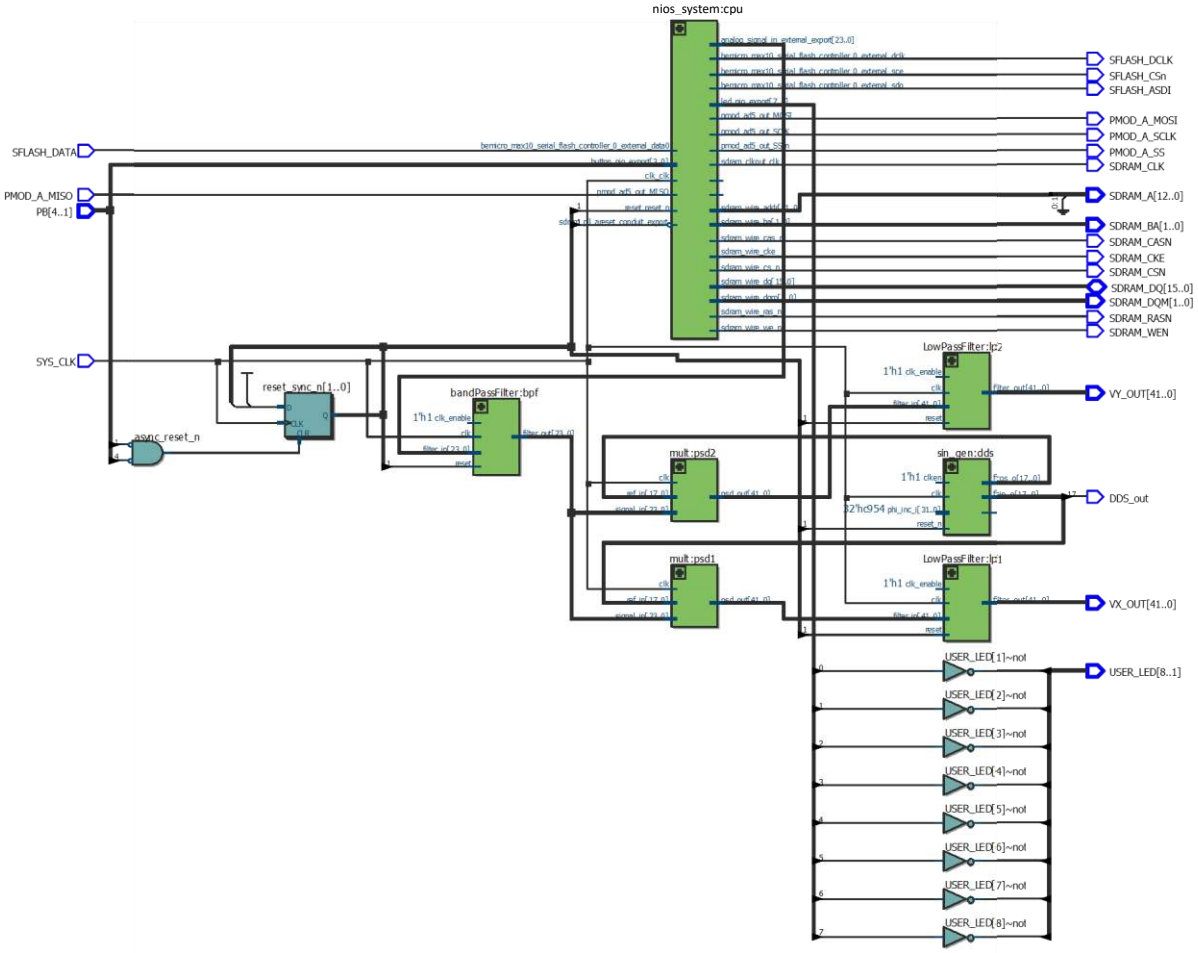

Fig. 8. RTL diagram for the complete system, after compilation.

IV. Conclusion

The present amplifier is intended to be part of a larger instrument for photorefractive and photoconductive materials characterization and should be able to measure photocurrents lower than 1pA in a large environment noise.

The final objective will be to include this lock-in amplifier into a larger instrument for characterizing photorefractive and photoconductive materials.

This work has provided a very good experience on synchronous demodulation and phase sensitive detection, which has many applications and will without a doubt be applied in future works and opportunities.

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References

[1] Stanford Research Systems. “Model SR830: DSP Lock-In Amplifier”. Rev. 2.5, 2011.

[2] C. He, L. Zhang, B. Liu, Z. Xu, Z. Zhang, A digital phase-sensitive detector for electrical impedance tomography, 2008 IEEE World Automation Congress, 1-4, 2008.

[3] A. Restelli, R. Abbiati, and A. Geraci , Digital field programmable gate array-based lock-in amplifier for high-performance photon counting applications, Review of Scientific Instruments 76, 093112-2, 2005.

[4] M. Davidovic, J. Seiter, M. Hofbauer, W. Gaberl, H. Zimmermann, Dual-lock-in sensor IC with integrated PIN photodetectors, Analog Integr Circ Sig Process (2014) 81:797–804, 2014.

[5] J.J. Vandenbussche, P. Lee, and J. Peuteman, On the Accuracy of Digital Phase Sensitive Detectors Implemented in FPGA Technology, IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 63, NO. 8, AUGUST 2014.

[6] Altera Wiki. “BeMicro Max 10”. http://www.alterawiki.com/wiki/BeMicro_Max_10

[7] Digilent. “PmodAD5: 4-channel 4.8 kHz 24-bit A/D Converter”. http://store.digilentinc.com/pmodad5-4-channel-4-8-khz-24-bit-a-d-converter/

[8] Analog Devices. “AD7193: 4-Channel, 4.8 kHz, Ultralow Noise, 24-Bit Sigma-Delta ADC with PGA”. Rev. D, 2013.

[9] Michael Clifford. “Fundamental Principles Behind the Sigma-Delta ADC Topology”. Analog Devices Technical Article. 2016.

[10] Quartus II Handbook Volume 3: Verification. “Design Debugging Using the SignalTap II Logic Analyzer”. Chapter 13, 2015.

[11] Mary McCarthy. “AN-0979: Digital Filtering Options: AD7190, AD7192”. Analog Devices Application Note, Rev. 0, 2009.

[12] Altera Corporation. “NCO IP Core User Guide”, 2014.